Chapter 3
The Switched Local Area Networks' Delay Problem: Issues and a Deterministic Solution Approach

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ABSTRACT

A large number of installed local area networks are sluggish in terms of speed of uploading and downloading of information. Researchers have, therefore, proposed the need for such networks to be designed with specified maximum end-to-end delay. This is because, if the maximum packet delay between any two nodes of a network is not known, it is impossible to provide a deterministic guarantee of worst case response times of packets' flows. Therefore, the need for analytic and formal basis for designing such networks becomes very imperative. In this regard, this chapter has discussed the switched local area networks' delay problem and related issues. It compared the two principal approaches for determining the end-to-end response times of flows in communication networks – stochastic approach and deterministic approach. The chapter goes on to demonstrate the superiority of the latter approach by using it to develop and validate the goodness of a general maximum delay packet switch model.

INTRODUCTION

The rapid establishments of standards relating to Local Area Networks (LANs), coupled with the development by major semi-conductor manufacturers of inexpensive chipsets for interfacing computers to them has resulted in LANs forming the basis of almost all commercial, research and university data communication networks. As the applications of LANs have grown, so are the demands on them in terms of throughput and reliability. (Halsall, 1992, p. 308) The literature on LANs

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is almost in a flux. However, a common challenge that has been confronting researchers for a long time now, is, how to tackle the problem of slow response of local area networks. Slow response of such networks means packets' flows from one host (origin host) to another host (destination host) takes longer time than is necessary for comfort at certain times of the day. In this regard, switched networks were quite recent developments by the computer networking community in attempts at solving this slow response challenge. While the introduction of switched networks have reduced considerably this slow response (and, hence, long delay) problem, it has not completely eliminated it. This has elicited researches into switched networks in efforts at totally eliminating this problem. These researches have been said to be important in the present dispensation because of the deployment and/or the increased necessity to deploy real-time applications on these networks. In the next and succeeding sections, theoretical concepts that are important for an understanding of the switched LANs' delay problem, and of some aspects of the solutions approaches that has been adopted by our research team are discussed. In this regard, the network calculus and traditional queuing approaches to modeling network traffic are compared and contrasted, and some elementary network components, which were proposed and characterized by Cruz (1991) are described. The chapter then went on to describe a maximum delay model of a packet switch, which, was shown to be good for the practical engineering of local area networks that meets specified maximum end-to-end delay constraints.

BACKGROUND

The design of switched networks has largely been based on experience and heuristics. Experience has shown that, the network is just installed, switches randomly placed as the need arises, without any load analysis and load computation; there are usually no performance specifications to be met. This approach, frequently leads to expensive systems that fail to satisfy end users in terms of speed in uploading and downloading of information (Kanem et al., 1999; Torab and Kanem, 1999). In other words, this approach, usually leads to long networks' delays. According to Gallo and Wilder (1981), in a network, the arrival of information in real-time to the destination point at a specified time is a critical issue. In the view of Fowler and Leland (1991), there are times when a network appears to be more congestion-prone (incurring long packets' delays) than at other times. Falaki and Sorensen (1992) has also once averred that, there have always been a need for a basic understanding of the causes of communication delays in distributed systems on a Local Area Network (LAN).

THE DELAYS IN COMPUTER NETWORKS

One fundamental characteristics of a packet-switched network is the delay required to deliver a packet from a source to a destination. (Bolot, 1993) Each packet generated by a source is routed to the destination via a sequence of intermediate nodes; the end-to-end delay is, thus, the sum of the delays experienced at each hop on the way to the destination. (Bolot, 1993) Each such delay in turn consists of two components (Ming-Yang et al., 2004; Bolot, 1993; Bertsekas and Gallager, 1992, p. 150);

1. A fixed component which includes:
   a. The transmission delay at the node,
   b. The propagation delay on the link to the next node,
2. A variable component which includes:
   a. The processing delay at the node,
   b. The queuing delay at the node.

Transmission delay is the time required to transmit a packet (Gerd, 1989, p. 110), it is the time between when the first bit and the last bit are transmitted. (Bertsekas and Gallager, 1992, p. 150) Propagation delay is the time between when the last bit is transmitted at the head node of a link and the time when the last bit is received at the tail node. (Bertsekas & Gallager, 1992, p. 150) Processing delay is the time required for nodal equipment to perform the necessary processing and switching (Comer, 2004, p. 244) of data (packets in packet switched networks) at a node. (Bertsekas & Gallager, 1992, p. 150; Gerd, 1989, p. 110) Included here are error detection and address recognition, and transfer of packet to the output queue. (Gerd, 1989, p. 110) Queuing delay is the time between when the packet is assigned to a queue for transmission and when it starts being transmitted; during this time, the packet waits while other packets in the transmission queue are transmitted. (Bertsekas & Gallager, 1992, p. 150) The queuing delay has the most adverse effect on packet delay in a switched network (Song, 2001).

Two other types of delays identified by Gerd (1989, p. 240), are, the waiting time at the buffers associated with the source and destination stations and the processing delays at these stations; this was called thinking time in (Jasperneite & Ifak, 2001). But these are usually not part of end-to-end delay (see previous definition of end-to-end delay), since in a way, by simply having hosts of high buffer and processing capacities, delays associated with the host stations can be minimized. Moreover, the capacities of host stations are not part of the factors that are put into consideration when engineering local area networks. As argued by Costa et al. (2004), the message processing time consumed in source and destination hosts is not included in the calculation of end-to-end delay because these times are not directly related to the physical conditions of the network. Access delays occur when a number of hosts share a medium and hence may wait in turns to use the medium (Comer, 2004, p. 244); but this delay does not apply to switched networks.

While propagation and switching delays are often negligible, queuing delay is not (Bertsekas & Gallager, 1992, p. 150; Ersoy & Panwar, 1993; Georges et al., 2005). Inter-nodal propagation delay is negligible for local area networks (Mann & Terplan, 1999, p. 247; Gerd, 1989, p. 110), propagation delays are neglected in delay computations even in wide area networks because of its negligibility. (Bertsekas & Gallager, 1992, p. 15) It is, therefore, reasonable to neglect propagation delays when computing end-to-end delays.

SWITCHED LOCAL AREA NETWORKS AND THE NETWORK DELAY PROBLEM

Local Area Networks made a dramatic entry into the communications scene in the late 1970s and early 1980s. (Bertsekas & Gallager, 1992, p. 2; Gerd, 1989, p. 13) The manner in which the nodes of a network are geometrically arranged and connected is known as the topology of the network and local area networks are commonly characterized in terms of their topology. (Bertsekas & Gallager, 1992, p. 146; Gerd, 1989, p. 50) A family of standards for LANs was developed by IEEE to enable equipment of a variety of manufacturers to interface to one another; this is called the IEEE 802 standard family. This standard defines three types of media-access technologies and the associated physical media, which, can be used for a wide range of particular applications or system objectives. (Bertsekas & Gallager, 1992, p. 54) The standards that relate to baseband LANs are the IEEE-802.3 standard for baseband CSMA/CD bus LANs, and IEEE 802.5 token ring local area networks. Several variations on IEEE 802.3 now exist. The original implementation of the IEEE 802.3 standard is the Ethernet system; this operates at 10Mb/sec. This original Ethernet, re-

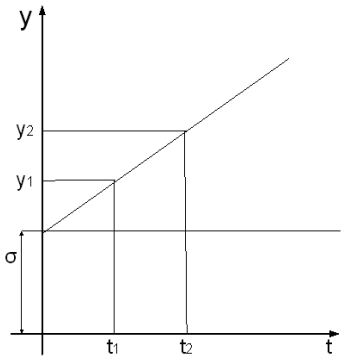
ferred to as Thicknet, is also known as the IEEE 802.3 Type 10-Base-5 standard. A more limited abbreviated version of the original Ethernet is known as Thinnet or Cheapernet or IEEE 802.3 Type 10-Base-2 standard. Thinnet also operates at 10Mb/sec, but uses a thinner, less expensive coaxial cable for interconnecting stations such as personal computers and workstations. A third variation originated from Star LAN, which was developed by AT&T and uses unshielded, twisted-pair cable which is often already installed in office buildings for telephone lines (Bertsekas & Gallager, 1992, p. 364; Michael & Richard, 2003, p. 220), and the first version was formally known as IEEE 802.3 Type 10-Base-T. There has been other versions of the twisted pair Ethernet – Fast Ethernet (100-Base-T or IEEE 802.3u), Gigabit Ethernet (1000-Base-T or IEEE 802.3z). Instead of a shared medium, twisted pair Ethernet wiring scheme uses an electronic device known as a hub in place of a shared cable; electronic components in the hub emulate a physical cable, making the entire system operate like a conventional Ethernet.

Ethernet, in its original implementation, is a branching broadcast communication system for carrying data packets among locally distributed computing stations. The thicknet, thinnet and hub-based twisted-pair Ethernet are all shared-medium networks. (Song, 2001) That is, traditional Ethernet (which these three types of Ethernet represent), in which all hosts compete for the same bandwidth is called shared Ethernet. Because access to the shared medium by the attached hosts' are random in nature, packets' collisions in the medium are inevitable. The Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol was therefore, developed to control access of the interconnected stations to the shared medium; but this result in a non-deterministic access delay, since, after every collision, a station waits a random delay before it retransmits. (Bolot, 1993) The probability of collision depends on the number of stations in a collision domain and the network load. (Georges et al., 2005; Song, 2001) Moreover, the number of stations attached to a shared-medium Ethernet LAN cannot be increased indefinitely; as eventually, the traffic generated by the stations will approach the limit of the shared transmission medium. (Alberto & Widjaja, 2004, p. 433) One traditional way to decrease the collision probability is to reduce the size of the collision domain by forming micro-segments separated by bridges (Song, 2001). This is where switches come in, as functionally, switches can be considered as multi-port bridges. (Bejerano, et al., 2003; Song, 2001)

A Switched Ethernet, therefore, is an Ethernet/802.3 LAN that uses switches to connect individual nodes or segments. On switched Ethernet networks where nodes are directly connected to switches with full-duplex links, the communications become point-to-point. That is, a switched Ethernet/802.3 LAN isolates network traffic between sending and receiving nodes. In this configuration, switches break up collision domains into small groups of devices, effectively reducing the number of collision (Georges et al., 2005; Song, 2001) Furthermore, with micro-segmentation with full-duplex links, each device is isolated in its own segment in full-duplex mode and has the entire port throughput for its own use; collisions are therefore, eliminate (Jasperneite & Ifak, 2001) The CSMA/CD protocol does not therefore, play any role in switched Ethernet networks (Anurag et al., 2004, p. 102). The collision problem is thus shifted to congestion in switches. (Georges et al., 2005; Song, 2001; Kanem et al., 1999) This is, because, switched Ethernet transforms traditional Ethernet/802.3 LAN from broadcast technology to a point-to-point technology. The congestion in such switches is a function of their loading (number of hosts connected) (Georges et al., 2005); in fact, loading increases as more people log on to a network (Falaki & Sorensen, 1992), and congestion occurs when the users of the network collectively demand more resources than the network can offer. (Bertsekas & Gallager, 1992, p. 27).

According to Trulove (2000, p. 143), LAN switching has done much to overcome the limitations of shared LANs; however, despite the vast

Figure 3. Graph of $y = \rho t + \sigma$



Clearly, from (3) and (4), $W\rho(R)(t) \leq \sigma$ for all t if and only if $R \sim (\sigma, \rho)$; $W\rho(R)(t)$ is the size of the backlog; that is, the amount of unfinished work at time t in a work-conserving system which accepts data at a rate described by the rate function R and transmits the data at rate ρ while there is data to be transmitted (work to be done). (Cruz, 1991)

BURSTY TRAFFIC AND NETWORK DELAYS

The class of message flows that satisfies the condition that, the amount of traffic in an interval is upper bounded by an affine function of the length of the interval has been found to be a useful class of models for traffic on internal links in networks that have to handle bursty traffic (Anantharam, 1993), and bursty traffic is one of the causes of congestion in a network.. (Forouzan, 2008, p.763) Congestion in a network may occur if the load on the network (the number of packets sent to the network) is greater than the capacity of the network (the number of packets a network can handle). (Forouzan, 2008, p. 763) Fundamentally, congestion occurs when the users of a network collectively demand more resources than the network (including the destination sites) has to offer (Bertsekas & Gallager, 1992, p. 27), and congestion leads to delays. (Bertsekas & Gallager, 1992, p. 27) Bursty traffic sessions, therefore, generally lead to large delays in networks (Bertsekas & Gallager, 1992, p. 511); the delay suffered in a switch by an arriving packet increases as the burstiness of the traffic going into the switch increases (Georges et al., 2003).

ELEMENTARY NETWORK COMPONENTS THAT CAN BE USED TO MODEL A PACKET SWITCH

This section discusses some elementary network components that can be used for the modeling of packet switches and is based on the work of Cruz (1991).

1. The Constant Delay Line

The constant delay line is a network element with a single input stream and a single output stream. The operation is defined by a single parameter D. All data which arrive in the input stream exit on the output stream exactly D seconds later; that is, each packet is delayed a fixed constant time before it is moved out. Thus, if Rin represents the rate of the input stream, then, Rout the rate of the output stream is given by Equation (6).

$$R_{out}(t) = R_{in}(t - D) \; for \; all \; t \qquad (6)$$

The maximum delay of a delay line is obviously D. The delay line can be used in conjunction with other elements to model devices that do not process data instantaneously. The constant delay line is illustrated in Figure 4.The routing latency in a packet switch could be modeled by applying a

In ATM systems, non-conformant data is either discarded, tagged with low priority for loss ("red" cells) or can be put in a buffer (buffered leaky bucket controller); with the Integrated Services Internet, non-conformant data is in principle, not marked, but simply passed as 'best effort' traffic (namely, normal IP traffic). (Le Boudec & Thiran, 2004, p. 10) A similar concept to the leaky bucket concept is the token bucket controller. While the leaky bucket algorithm shapes bursty traffic into fixed-rate traffic by averaging the data rate, the token bucket algorithm allows bursty traffic at a regulated maximum rate (Forouzan, 2008, p. 779).

TRAFFIC STREAM CHARACTERIZATION

In the network calculus approach for describing network traffic, a traffic stream (which is a collection of packets that can be of variable length [Cruz, 1991]) or flow is described by a wide-sense increasing function r(t). The function r is wide-sense increasing if and only if $r(s) \leq r(t)$ for all $s \leq t$. We represent a traffic stream as follows: for any $t > 0$,

$r(t) = \int_0^t R(s)\,ds$ is the amount of bits seen in the flow in the interval [0, t]. R(s) is called the rate function of the traffic stream (Le Boudec and Thiran, 2004, p. 9; Cruz, 1991); it is the instantaneous rate of traffic from the stream at time s. By convention, we take $r(0) = 0$ (Le Boudec and Thiran, 2004, p. 4).

Also, in this traffic modeling approach, for any $y \geq x$, $\int_x^y R(s)\,ds$ represents the amount of traffic seen in the flow in the time interval [x, y]. We note explicitly that the interval of integration is a closed interval.

DEFINITION OF BURSTINESS CONSTRAINT

According to Cruz (1991), given any $\rho \geq 0$ and $\sigma \geq 0$, $R \sim (\sigma, \rho)$ if and only if for all x, y satisfying $y \geq x$, there holds;

$$\int_x^y R \leq \sigma + \rho(y - x) \tag{2}$$

Thus, if $R \sim (\sigma, \rho)$, there is an upper bound on the amount of traffic contained in any interval [x, y] that is equal to a constant σ plus a quantity that is proportional to the length of the interval. The constant of proportionality ρ determines an upper bound to the long-term average rate of traffic flow, if such an average rate exists. For a fixed value of ρ, the term σ allows for some burstiness. (Cruz, 1991) From (2), another interpretation of the constraint $R \sim (\sigma, \rho)$ is that;

$$\int_x^y R - \rho(t - s) \leq \sigma \tag{3}$$

or

$$\sigma \geq \int_x^y R - \rho(t - s) \tag{4}$$

Therefore, a useful interpretation of the constraint $R \sim (\sigma, \rho)$ is as follows (Cruz, 1991): for any function R and a constant $\rho > 0$, define the function $W\rho(R)$ for all times by Equation (5).

$$W\rho(R)(t) = \max_{s \leq t}\left[\int_s^t R - \rho(t - s)\right],\ -\infty < t < \infty \tag{5}$$

pattern of arrivals in the stream (arriving instants and the number of bits in the arriving packets) and in the case of a link, on the way the link transmits packets from the stream (the link may be shared in some way between two or more packet streams). To analyze such situations, we use mathematical models that are variously called traffic models, congestion models, or queuing models. (Anurag et al., 2004, p. 120)

The modeling of network traffic is traditionally done using stochastic models (Georges et al., 2005; Bertsekas & Gallager, 1992, p. 149); for example, Bernoulli arrival process was assumed in (Song, 2001). But in order to guarantee bounded end-to-end delay for any traffic flow, the traffic itself has to be bounded. (Georges et al., 2003) This is where the arrival curve concept of traffic arrivals to a system is important. In integrated service networks (ATM and other integrated service internet), the concept of arrival curves is used to provide guarantees to data flows. (Le Boudec & Thiran, 2004) In this approach (arrival curve), the traffic is unknown, but it is assumed that its arrival satisfies a time constraint. Generally, this means that the quantity of data that has arrived before time t will not be more than the arrival curve value at time t. The constraints are normally specified by a regulation method; for example, the leaky bucket controller (regulation).

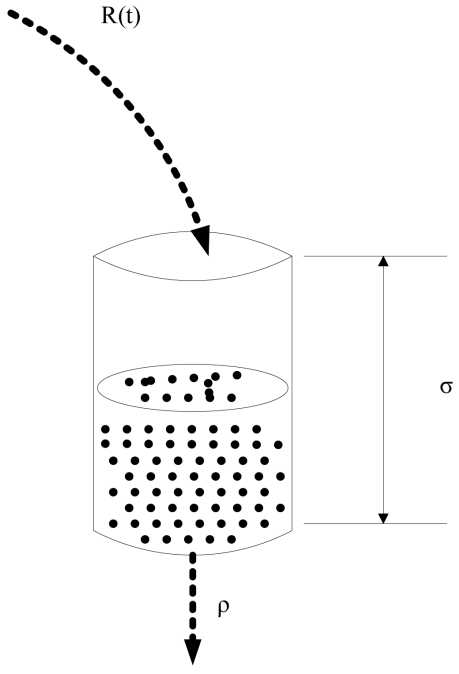
LEAKY BUCKET CONTROLLER

The arrival curve concept can be viewed as an abstraction of the regulation algorithm, and the most common example of traffic regulation algorithm is the leaky bucket algorithm, which has an arrival curve given by Equation (1) (Krishna et al., 2004);

$$b(t) = \sigma + \rho t \text{ for } t > 0, \quad (1)$$

which means that, no more than σ data units can be sent at once and the long-term rate is ρ. The arrival curve, therefore, bounds traffic and denotes the largest amount of traffic allowed to be sent in a given time interval. (Krishna et al., 2004; Bertsekas & Gallager, 1992, p. 512) A leaky bucket controller according to Le Boudec and Thiran (2004, p. 10) is a device that analyses the data on a flow as follows. There is a pool (bucket) of fluid of size σ. The bucket is initially empty. The bucket has a hole and leaks at a rate, ρ units of fluid per second when it is not empty. Data from the flow R(t) has to pour into the bucket an amount of fluid equal to the amount of data that will make the bucket to be full. Data that would cause the bucket to overflow is declared as non-conformant (it would not pour into the bucket) otherwise, the data is declared as conformant. The leaky bucket scheme is used to regulate the burstiness of transmitted traffic. (Bertsekas & Gallager, 1992, p. 911) Figure 2 is an illustration of the operation of the leaky bucket regulator, while Figure 3 illustrates it graphically.

Figure 2. Illustration of the leaky bucket controller concept



MODELING OF TRAFFIC FLOWS IN COMMUNICATION NETWORKS FOR NETWORK DELAY COMPUTATION PURPOSES: NETWORK CALCULUS VERSUS TRADITIONAL QUEUING THEORY

To determine the end-to-end response time of flows in a communication network two general approaches can be used: stochastic approaches or deterministic approaches. Stochastic approaches consist in determining the mean behavior of the considered network, leading to mean statistical or probabilistic end-to-end response times; while deterministic approaches are based on a worst-case analysis of the network behavior, leading to worst-case end-to-end response times. (Georges et al., 2005; Martin et al., 2005) This is because, stochastic processes are processes with events that can be described by probability functions; while a deterministic process is a process whose behavior is certain and completely known. Network calculus is a deterministic approach to modeling network entities and flows, while, queuing theory has traditionally been used for the same purpose. The advantages of the Network Calculus over the Traditional Queuing Theory can be put in the following compact form (Jasperneite et al., 2002; Bertsekas & Gallager, 1992, p. 149; Reiser, 1982):

NETWORK CALCULUS

1. Network calculus basically considers networks of service nodes and packets' flows between the nodes.
2. Network calculus involves bounded constraints on packets arrivals and services.
3. These bounded constraints allow bounds on the packets' delays and work backlogs to be derived, which can be used to quantify real-time network behavior.
4. The packets arrival processes in network calculus are described with the aid of arrival curves, which quantify constraints on the number of packets or the number of bits of a packet flow in a time interval at a service node.

TRADITIONAL QUEUING THEORY

1. Traditional queuing theory deals with stochastic processes and probability distributions.
2. Traditional queuing theory normally yields mean values and perhaps quantiles of distributions.
3. The derivations of these mean values and quantiles of distributions are often difficult.
4. Upper bounds on end-to-end delays may not exist or be computable.

Generally, the deterministic methodology which the network calculus represents considers the worst case performance of the network and, therefore, yields conservative results. (Anurag et al., 2004, p. 127) Network calculus has traditionally been used for scheduling and traffic regulation problems in order to improve Quality of Service (QoS); but it is now more and more being used to study switched Ethernet networks. (for example, Georges et al., 2005, 2003, 2002; Jasperneite et al., 2002) Network calculus can be used to engineer Internet networks. (Jasperneite et al., 2002) In end-to-end deterministic network calculus approach, input processes are characterized via envelops, network elements are characterized via service curves, and it is useful for the engineering of networks if worst-case guarantees are required. (Anurag et al., 2004, p. 252)

NETWORK TRAFFIC MODELING: THE ARRIVAL CURVE APPROACH

The delays experienced by packets of a given packet stream at a link or switch, depends on the

increase in bandwidth provision per user that this represents over and above a shared LAN scenario, there is still contention in the network leading to unacceptable delay characteristics. For example, multiple users connected to a switch may demand file transfers from several servers connected via 100 Mb/sec Fast Ethernet to the backbone. Each Server may send a burst of packets that temporarily overwhelms the Fast Ethernet uplink to the wiring closet. A queue will form in the backbone switch that is driving this link and any voice or video packet being sent to the same wiring closet will have to wait their turn behind the data packets in this queue. The resultant delays will compromise the perceived quality of the voice or video transmission.

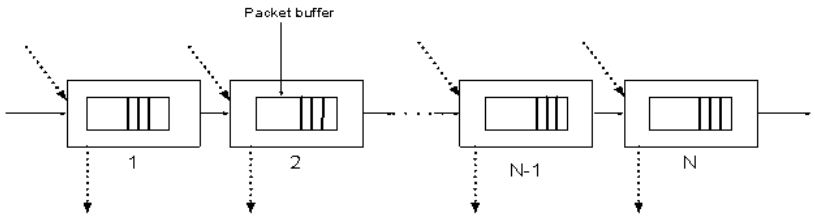
MITIGATING THE EFFECTS OF THE SWITCHED LOCAL AREA NETWORKS' DELAY PROBLEM

The path transversed by a packet through a network can be modeled as a sequence of queuing system (Alberto & Widjaja, 2004, p. 539; Torab & Kanem, 1999); this is illustrated in Figure 1. The dashed arrows show packets from other flows that may 'interfere' with the packet of interest in the sense of contending for buffers and transmission along the path. It should be noted that these interfering flows may enter at one node and depart at some later node, since they belong to different origin-destination pairs and follow different paths through the network.

The performance experienced by a packet along the path is the accumulation of the performances experienced along the N queuing systems; for example, the total end-to-end delay is the sum of the individual delays experienced at each system. (Alberto & Widjaja, 2004, p. 539) If we can guarantee that the delay at each system can be kept below some upper bound, then the end-to-end delay can be kept below the sum of the upper bounds. (Alberto & Widjaja, 2004, p. 540)

It is easy to see from Figure 1 that, a reasonable way to mitigate the effects of network delay problem on a switched LAN is to upper bound the end-to-end packet delay of each origin-destination path. The reason for this is that, if the end-to-end packet delay of a given network is upper bounded, then under no network loading condition will a packet's end-to-end delay exceed the upper bound. Therefore, to determine the maximum end-to-end delays from all origins to all destinations of a switched communication system (a path is illustrated in Figure 1), we must add the different maximum delays at each switch from all origins to all destinations if we know the number of switches on each route from origin to destination. (Alberto & Widjaja, 2004, p. 539; Torab & Kanem, 1999) Therefore, all we need to do in order to make this to be possible, is, to develop a maximum packet delay model for an arbitrary N-port packet switch.

Figure 1. The end-to-end QoS of a packet switch along a line transversing N queuing systems (source: Alberto & Widjaja, 2004, p. 539)



burst-delay service curve δT(t), which is equivalent to adding a constant delay T. (Georges et al., 2005) Figure 5a shows the input and output curves of the guaranteed delay element, while Figure 5b shows the curve of the burst-delay function.

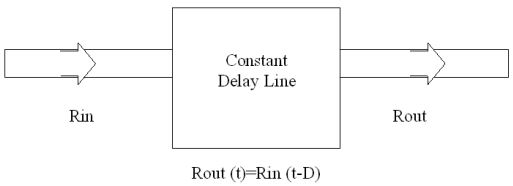
2. The Receiver Buffer

The receiver buffer is a network element with a single input stream and a single output stream. The input stream arrives on a link with a finite transmission, rate, say C. The output stream exits on a link with infinite transmission rate. The receiver buffer simply outputs the data that arrives on the input link in First-Come-First-Served (FCFS) order. The data packet exits the receive buffer instantaneously at the time instant when it is completely transmitted to the receive buffer on the input link. That is, the receive buffer does not output a packet until the last bit of the packet has been received; at which time, it now outputs the packet. The receive buffer is employed to model situations in which cut-through switching is not used; but, in which store-and-forward switching is used.

If Lk = length in bits of packet k that starts transmission on the input link at time Sk, then tk, the time at which the kth packet starts exiting the receive buffer is given for all k by Equation (7).

$$t_k = S_k + L_k \; / \; / \; C \qquad (7)$$

Figure 4. Illustration of a constant delay line



Obviously, the maximum delay of any data bit passing through this network element is upper bounded by L/C, and the backlog in the receive buffer is obviously bounded by L. The receiver buffer is a useful network element for modeling network nodes, which must completely receive a packet before the packet commences exit from the node. For example, the receiver buffer is a convenient network-modeling element in a data communication network node that performs error correction on data packets before placing them in a queue. In addition, the receive buffer is useful for devices in which the input links have smaller transmission rates than the output links. The receive buffer is illustrated in Figure 6.

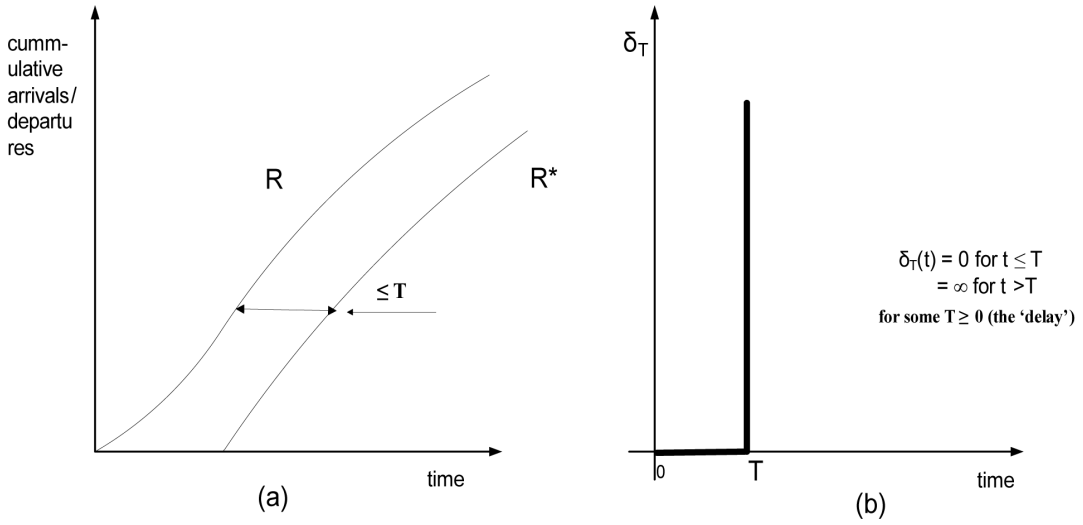
3. The First-Come-First-Served Multiplexer (FCFS MUX)

The multiplexer (FCFS MUX) has two or more input links and a single output link. The function of the FCFS MUX is to merge the streams arriving on the input links onto the output link. That is, it multiplexes two or more input streams together onto a single output stream. The output link has maximum transmission rate Cout and the input links have maximum transmission rates Ci, i = 1,2,3,…,N. It is normally assumed that Ci ≥ Cout, for i = 1, 2, 3,…,N. An illustration of the FCFS MUX is shown in Figure 7.

4. First-In-First-Out (FIFO) Queue

The FIFO queue can be viewed as a degenerate form of FCFS multiplexer. The FIFO queue has one input link and one output link. It is illustrated in Figure 8. The input link has transmission capacity Cin and the output link has transmission capacity Cout. The FIFO is defined simply as follows. Data that arrives on the input link is transmitted on the output link in FCFS order as soon as possible at the transmission rate Cout. For

Figure 5. Illustration of arrivals delayed for at most T seconds before departure (input/output curves of guaranteed delay elements) (a) and the burst-delay function δ, (b) Source: LeBoudec & Thiran (2004, p. 107)

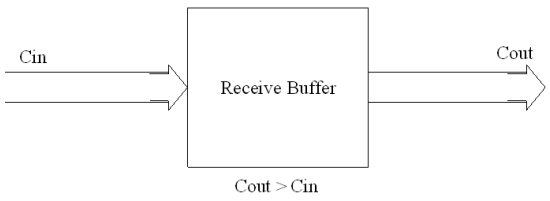


example, if a packet begins to arrive at time t0 and if no backlog exists inside the FIFO at time t0, then the packet also commences transmission on the output link at time t0. It is assumed that Cin ≥ Cout so that this is possible. If Cin were less than Cout, then this would be impossible to do, as the FIFO would 'run out' of data to transmit immediately following time t0 before the packet could be transmitted at rate Cout. Suppose that the rate of the input stream to the FIFO queue is given as Rin(t), if the size of the backlog inside the FIFO at time t is given by WCout (Rin)(t). The jth packet which arrives at time Sj must wait for all, the, current backlog and this backlog gets transmitted at rate Cout. It follows that the jth packet commences exit from the FIFO queue at time tj = Sj + dj, where,

$$d_j = \frac{1}{Cout} W_{Cout}(R_0)(S_j) \tag{8}$$

= time spent by the jth packet in the FIFO queue before being transmitted at rate Cout.

Figure 6. Illustration of a receive buffer



MAXIMUM DELAY MODEL OF A PACKET SWITCH

A switch is a complex system which introduces different mechanisms and different technologies. (Georges et al., 2005, 2003) Some researchers have modeled a packet switch as a black box (for example Jasperneite et al., 2002); the service curve notion defined in (Le Boudec & Thiran, 2004, p. 18) was also used in (Jasperneite et al., 2002) to describe the service offered by a switch to packets that are arriving to it. We now proceed

Figure 7. Illustration of a FCFS MUX

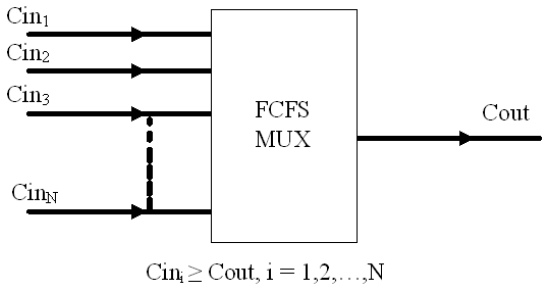
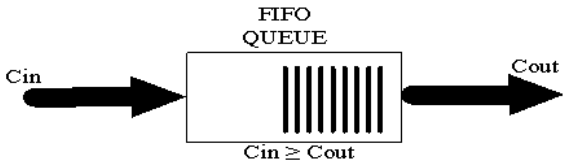


Figure 8. Illustration of a FIFO queue



in the next few sections to describe a maximum delay model of a packet switch developed by using the elementary components whose operations were explained in paragraph titled "The Receiver Buffer" and to derive its mathematical equivalent. The model is shown in Figure 9.

DESCRIPTION OF THE MAXIMUM DELAY MODEL

The maximum delay packet switch model is based on the following delays/latencies: (1) packet (frame) forwarding latency, (2) packet (frame) routing latency, (3) queuing delay, (4) packet (frame) transmission delay and, (5) concurrent arrival of packets (frames) delay. So the maximum delay, which a packet will suffer in a packet switch is given by:

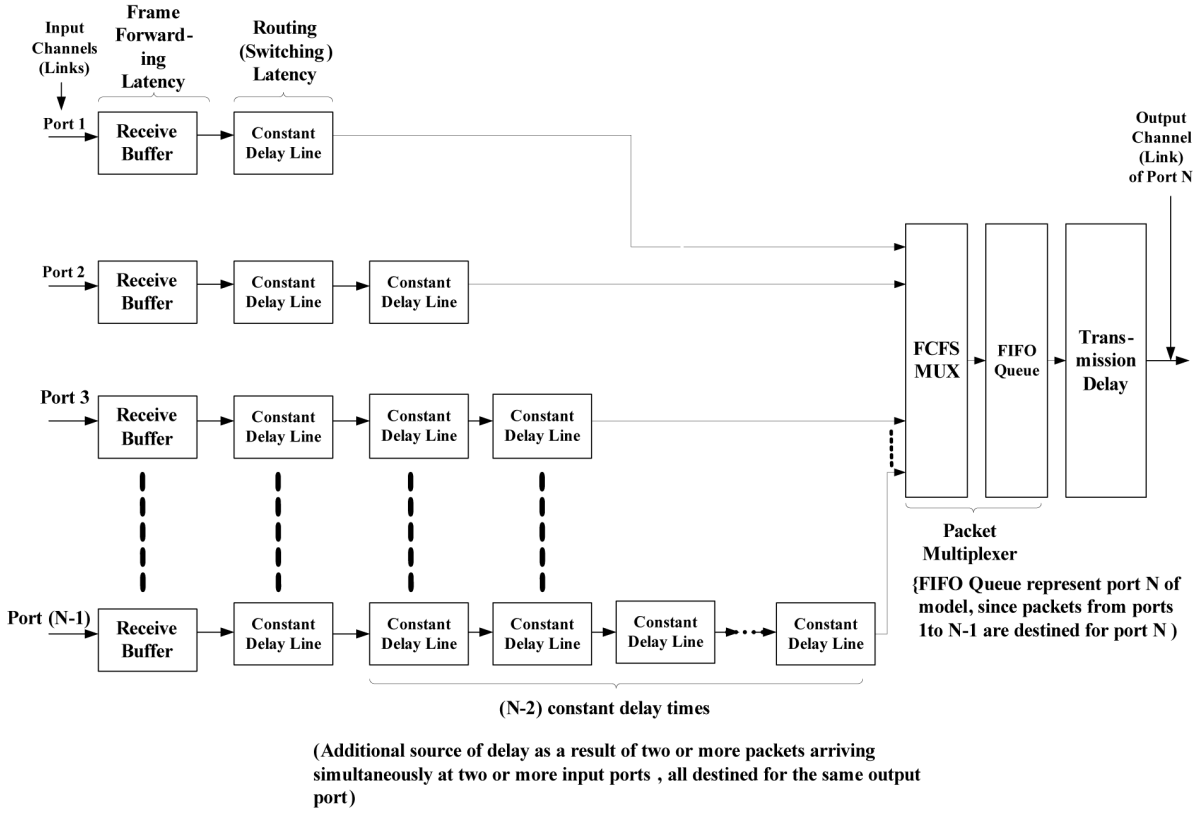
Maximum Packet Delay = Maximum Forwarding (Store and Forward) Latency + Maximum Routing (Switching) Latency + Maximum Delay as a result of concurrent arrival of packets + Maximum Queuing Delay + Maximum Transmission Delay (9)

In the model, there, are, N-1 (where N is the number of ports in the switch) receive buffers, representing the input buffering at each of the input ports of packet switches. Christensen et al. (1995) emphasized the need for input buffering in LAN switches when they averred that, a LAN switch must ensure that frames from two or more simultaneously transmitting workstations are not lost due to contention (they can be contending for the same output port) within the switch; LAN switches, therefore, usually contain both input and output ports buffering.

Next, there are N-1 constant delay lines. These constant delay lines are each used to model the routing (switching) latency of a packet in the switch. They are also used to model the delay suffered by one or more packets in a packet switch when two or more packets arrive at input ports simultaneously, and all of these arriving packets are destined for the same output port. When two packets arrive simultaneously at two input ports, but both of them are destined for the same output port, one of them is delayed for a fixed constant time (T seconds) before it is sent to the output port.

Then, there are a set of constant delay lines between the first set of constant delay lines and the FCFS MUX (first-come, first-serve multiplexer). The first port (port 1) has no other constant delay line (except the constant delay line that is used to model routing or switching latency). The second port (port 2) has one constant delay line, the third port has two constant delay lines, and so on up to the (N-1)th port that has N-2 constant delay lines between the constant delay line that models the routing (switching) latency and the FCFS MUX. These set of constant delay lines are necessary because, the switch model is a maximum packet delay model. These constant delay lines, therefore, model a part of the packet switch maximum delay as follows. It is known that N-1 packets can arrive simultaneously at N-1 input ports all destined for the Nth output port. Therefore, one will have to be the first to be sent to the output port. It is assumed that the data packet that

Figure 9. Maximum delay model of a packet switch



arrived at port 1 is the first to be sent to the port N; therefore, it suffers no delay. Then the packet that arrived at port 2 is the next to be sent to the output port N, therefore, it suffers one delay (represented by the one constant delay line). The packet that arrived at port 3 is the next to be sent to output port N, therefore, it suffers two delays (represented by the two constant delay lines), and so on up to the packet that arrived at port N-1 being the next to be sent to output port N, therefore, it suffers N-2 delays (which is represented by N-2 constant delay lines).

The next component in this model is the FCFS MUX (first come, first serve multiplexer).The multiplexer has two or more input links and a single output link. The function of the MUX is to merge the streams arriving on the input links onto the output link. It is included in the model to indicate the fact that, packets can arrive at different input ports (represented by the inputs of the multiplexer), but all of them are destined for the same output port (the output of the multiplexer).

FIFO (first-in, first-out) Queue is the next component in the model. It is used to model the output queuing in packet switches. If a data packet arrives at the input port, after the packet header has been checked to know its destination address, it is switched (routed) to the output port corresponding to the destination address by the switching fabric. If there are other packets waiting in the queue of the output port to be transmitted on the transmission line, it has to wait for the transmission of these other data packets before being transmitted. The FCFS MUX together with the FIFO queue is called packet multiplexer (this is because, apart from multiplexing data packets

from multiple inputs onto a single output, data multiplexers contain buffers for queuing data packets). The last component in the model is a unit that models the transmission delay in a switch (that is, the delay between when the first bit of a packet is placed on the transmission line that is attached to the output port and when the last bit of the packet is placed on the same transmission line).

MATHEMATICAL EQUIVALENT OF THE MAXIMUM DELAY MODEL OF A SWITCH

We now proceed to obtain the equivalent mathematical model for this maximum delay packet switch model. It should explicitly be noted here that, the basic assumption of this model is that, it is the packet that arrives at the (N-1)th input port that will suffer the maximum delay in the switch.

RECEIVE BUFFER

A packet of length L-bits arriving over a link of bit rate Ci, has a maximum delay given by Equation (10). (Anurag et al., 2004, p. 121; Cruz, 1991)

$$\text{Dbuffer} = \frac{L}{C_i}\,(\text{secs}) \tag{10}$$

CONSTANT DELAY LINE

This switch model is assumed to be based on the shared-memory switching fabric, which is the most commonly implemented switching fabric for local area network switches (Georges et al., 2005). In this type of switch, the packets transfer rate of the switching fabric is usually at least twice the sum of the input line rates. (Anurag et al., 2004, p. 600; Song, 2001) Therefore, assuming that there are N ports with input line rates x1, x2, x3,…,xN in bps (bits per second) = speeds of the connected mediums to input ports 1, 2, 3,…,N of the switch = input rates (ci's) of the receive buffers; if SFTR = switching fabric transfer rate, then, SFTR $\geq$ [2×(x1+x2+x3+ …+xN)]bps; which, taking the lower bound, gives;

SFTR = [2× (c1+c2+c3+ …+cN)]bps

$$= [2\times (\sum_{i=1}^{N} c_i)]\ \text{bps} \tag{11}$$

But Cruz (1991) contends that the operation of a constant delay line is described by a single parameter D, and that all data that arrive in the input stream exit in the output stream exactly D seconds later. We can then say that one packet delay time in seconds is that shown in Box 1.

Then the delay D in seconds of a packet in a constant delay line becomes:

$$D\left(\text{secs}\right) = \left(\frac{L}{2\times\sum_{i=1}^{N} C_i}\right) \tag{12}$$

Since the arriving (N-1)th packet will suffer N-2 constant delay times in this model, we then have:

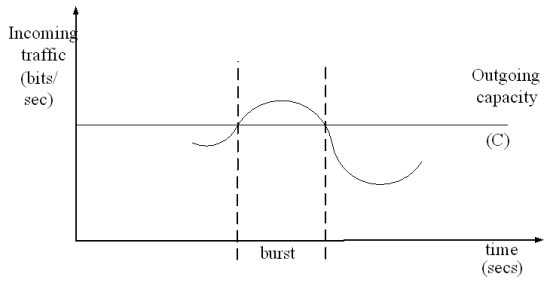
$$D_{CDT}\left(\text{secs}\right) = \left(N-2\right)\times\left(\frac{L}{2\times\sum_{i=1}^{N} C_i}\right) \tag{13}$$

where, DCDT = maximum delay suffered by a data packet in the switch as a result of N-1 constant delay times,

N = the number of I/O ports in the switch,

L = maximum length in bits of a data packet.

Figure 12. Illustration of traffic arrivals to, and departures from, a queuing system with constant output rate, C (Source: Sven, et al., 2008)



packet that arrived in port N-1 will suffer the maximum delay – it is the last to be forwarded to the output port N), we have Equation (35) in Box 3.

PRACTICAL IMPLICATIONS OF THE MAXIMUM DELAY MODEL OF A PACKET SWITCH

It is easy to see from Figure 1 that, if one can guarantee that the delay of a packet in any of the switches in an origin-destination path can be kept below an upper bound, then the end-to-end delay of the path can be kept below the sum of the upper bounds delays of the switches on that path. If we are able to know all the origin-destination paths in any switched LAN (this can be done with a methodology that we have developed in our research work), with our maximum delay model of a packet switch, we can calculate all the origin-destination paths maximum delays. We can then go ahead to compare these maximum delays with the maximum delay constraints of the applications to be deployed in the LAN. If the origin-destination paths maximum delays are all below the maximum delay constraints of the applications to be deployed in the LAN, then the network is well designed; if otherwise, then the network has to be redesigned so as to have maximum paths end-to-end delays that are below the maximum delay constraints of the applications. Consequently, the maximum delay packet switch model was validated to be good for practical network engineering by comparing its maximum delay value to values that were obtained

Box 3.

$$D_{\max}\left(\text{seconds}\right) = \frac{L}{C_{N-1}} + \left(\frac{L}{2\times\sum_{i=1}^{N} C_i}\right) + \left(N-2\right)\times\left(\frac{L}{2\times\sum_{i=1}^{N} C_i}\right) + \frac{\sigma}{C_{out}} + \frac{L}{C_{out}}$$

$$= \frac{L}{C_{N-1}} + \left(N-1\right)\times\left(\frac{L}{2\times\sum_{i=1}^{N} C_i}\right) + \frac{\sigma}{C_{out}} + \frac{L}{C_{out}} \qquad (35)$$

where,
Dmax = maximum delay in seconds for a packet to cross any N-port packet switch,
N = No of input/output ports,
Ci, i = 1, 2, 3,…,N = bit rates of ports 1, 2, 3,…,N in bps,
= channel (for example, Ethernet) rates of input ports in bps,
Cout = bit rate of the Nth output link in bps,
= output port (line) rate of the Nth port (the destination of the other N-1 input traffics)
CN-1 = bit rate of the (N-1)th input port in bps,
L = maximum length in bits of a data (for example, Ethernet) packet,
σ = maximum amount of traffic in bits that can arrive in a burst.

Box 2.

$$d_j = \frac{1}{C_{out}}\left[C\left(\frac{\sigma}{C-\rho}\right) - C_{out}\left(\frac{\sigma}{C-\rho}\right)\right] = \frac{1}{C_{out}}\left[\frac{(C-C_{out})\,\sigma}{C-\rho}\right] \quad (32)$$

= maximum delay in seconds incurred by the jth packet in crossing the FIFO queue.

Therefore, taking ρ as Cout, Equation (32) becomes:

$$d_j = \frac{\sigma}{C_{out}} \quad (33)$$

where,

d j = maximum delay in seconds incurred by the jth packet in crossing the FIFO Queue,
σ = maximum amount of data traffic that can arrive in a burst in bits,
Cout = bit rate of the output link (switch port) in bits per second (bps).

Equation (33) is in agreement with the assertion (with respect to a router) by Sven et al. (2008), that since the output queue of a router is emptied at the nominal link capacity, an hypothesis can be made that, the size of a packet burst in bits measured on a router's output port divided by the nominal physical link capacity is the upper limit of delay added to the queue build-up by the packet burst.

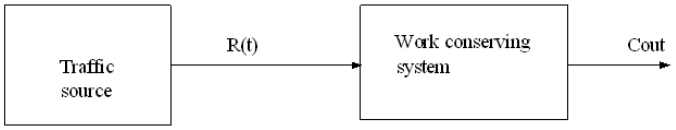
TRANSMISSION DELAY

According to Kanem et al. (1999), Bersekas and Gallager (1992, p. 149), Gerd (1989, p. 169) Reiser (1982), for all arriving instants, the delay experienced by a message upon arrival at a queuing system is composed of the message's own service time plus the backlog 'seen' upon arrival. The maximum transmission delay that can be suffered by an arriving packet is obviously the ratio of the maximum size that can be assumed by the packet to the transmission speed of the output port (channel). Therefore, if L = maximum length of a packet in bits, Cout = transmission speed of the output port (link) in bits/sec, Dmaxtrans, the maximum transmission delay of the packet in the switch in seconds is given by Equation (34).

$$D_{\text{maxtrans}} = \frac{L}{C_{out}} \text{ secs} \quad (34)$$

We can then insert the maximum delay expressions of Equations (10), (13), (33), and (34) into Equation (9) and by replacing Ci in Equation (10) by CN-1 (since we have assumed that the data

Figure 11. Traffic source sending data at a time dependent rate R(t) to a work conserving system, that issues out the traffic at a constant rate, Cout



Box 1.

$$D\left(\text{secs}\right) = \frac{packet\ \ length\ \ (bits)}{packet\ transfer\ rate\ \ (bits\ /\ \sec s)} = \frac{L\ \ (bits)}{packet\ transfer\ rate\ \ (bits\ /\ \sec s)}$$

that is

$$C(sj-s)=\sigma+\rho(sj\ -s) \tag{30}$$

or

$$S_j - S = \frac{\sigma}{C-\rho} \tag{31}$$

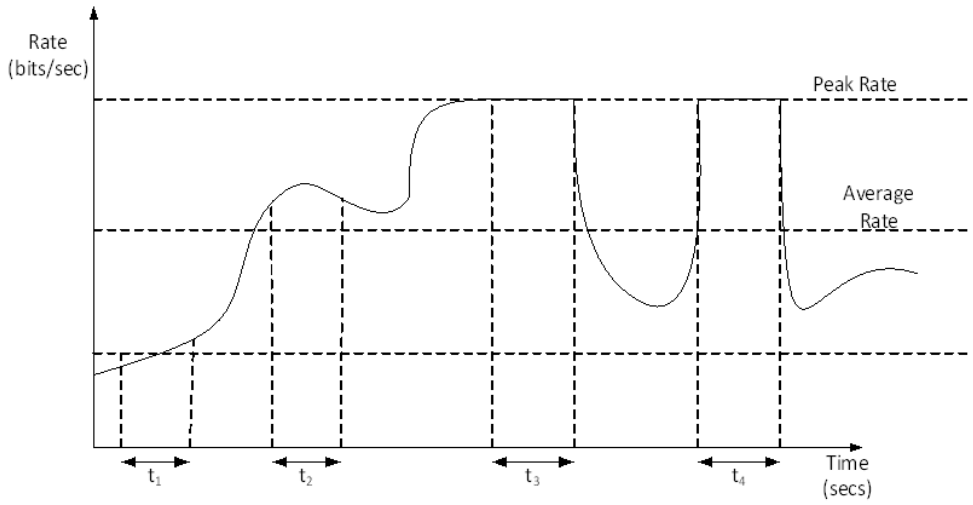
= maximum length of time at which the traffic flows at the peak rate.

We can now re-write Equation (27) as Equation (32) in Box 2.

We note here again that σ is the maximum amount of traffic (in bits) that can arrive in a burst to the FIFO Queue. But we had earlier stated that ρ is the rate at which a work-conserving system that accepts data at a rate described by the rate function R, transmits the data while there is data to be transmitted (Cruz, 1991). We can explain this concept in this simple way. Consider a work-conserving system as shown in Figure 11, which receives data at a rate described by R(t) and issues out the data at a constant rate Cout. Consider also, a communication session between the traffic source and the work-conserving system. It is easy to see that the traffic that arrives to the work-conserving system during the communication session (including burst traffic arrivals) would eventually be issued out by the system over time, at, rate Cout. It is easy to see also, that, Cout represents the average rate of traffic arrivals to the work-conserving system during the communication session.

This idea (output port issuing rate equals average rate of traffic arrivals) was amply illustrated by Sven et al. (2008) as shown in Figure 12.

Figure 10. An example of traffic arrival pattern to a queuing system



$$b(t)=\sigma+\rho t \tag{18}$$

where, b(t) is an affine arrival curve. In consonance with the description of the physical layer switch system in (US Patent No. 5889776, 2008); that the switching circuit of a switch establishes a link between two ports specified by the source address and the destination address that is received from the status look-up table, we can then take into account, the internal bus (the bus connecting the receive buffer to the output buffer) capacity (transfer rate). If this is C bits/sec, then the affine function (Equation [18]) can be completed with an inequality constraint as:

$$b(t)\leq Ct \tag{19}$$

This inequality constraint idea was introduced by Georges et al. (2005) in relation to the communication link feeding a switch. The inequality relationship represented by (19) means that, the arrival of data to the output buffers cannot be greater than the internal bus capacity through which the data will flow. Equation (18) can now be completed with the inequality constraint (19) as:

$$b(t) = \min\left\{ C\,t, \sigma+\rho\,t\right\} \tag{20}$$

We can now write out the amount of data that have arrived in the interval [sj, s] for all sj ≥ s as:

$$\int_{S}^{S_j} R_{in}(t)dt \leq \min\left\{C(s_j-s), \sigma+\rho(s_j-s)\right\} \tag{21}$$

From Equation (20), if $Ct<\sigma+\rho t,$ then

$$b(t)=Ct\,and \tag{22}$$

$$\frac{db(t)}{dt}=C \tag{23}$$

and if $\sigma+\rho t< Ct,$ then

$$b(t)=\sigma+\rho t \text{ and } t> \tag{24}$$

$$\frac{db(t)}{dt}=\rho \tag{25}$$

Equations (23) and (25) then give us two possible arrival rates: C, the internal bus capacity and ρ, a long term average rate (both are in bits/sec). But the maximum burst size has been defined as the maximum length of time that a data traffic flows at the peak rate. (Forouzan, 2008, p.762; Alberto & Widjaja, 2004, p. 551) We, therefore, ignore Equation (25) which deals with average rate. Equation (21) can now be written (taking the upper bound of the inequality) as:

$$\int_{S}^{S_j} R_{in}(t)\,dt = C\ (s_j-s) \tag{26}$$

Equation (16) now becomes:

$$d_j = \frac{1}{C_{out}} = \max_{s \leq s_j}\left[C(s_j-s)-C_{out}(s_j-s)\right] \tag{27}$$

To determine the maximum length of time or max [sj – s] that the incoming traffic flows at the peak rate, we note that, the upper bound of the inequality of (21) implies, either

$$\int_{S}^{S_j} R_{in}(t)\,dt = C\ (s_j-s) \tag{28}$$

or

$$\int_{S}^{S_j} R_{in}(t)\,dt = \sigma+\rho\ (s_j-s) \tag{29}$$

The ci's are the input rates of the receive buffers.

FIRST-COME-FIRST-SERVED MULTIPLEXER (FCFS MUX)

The multiplexer is assumed to be bufferless. We adopt the notion in this presentation that, output contention resolution (packet scheduling policy) along with output buffering (used for output queuing), both in the switch is called packet multiplexer. (Anurag et al., 2004, p. 120). Packets, therefore, do not suffer delay in the FCFS MUX. The delay that is supposed to be suffered by packets in the FCFS MUX is represented by the succeeding FIFO Queuing delay.

FIRST-IN-FIRST-OUT (FIFO) QUEUE

Wρ(R)(t), the size of the backlog (amount of unfinished work) at time t in a work-conserving system which accepts data at a rate described by the rate function R, and transmits data at the rate ρ while there is work to be done (data to be transmitted) was defined by Cruz (1991) as:

$$W_{\rho}\left(R\right)\left(t\right) = \max_{s \le t}\left[\int_{s}^{t} R - \rho(t-s)\right] \qquad (14)$$

where, ρ is an upper bound on the long-term average rate of traffic flow, and σ is the burstiness constraint of the traffic flow (and also the maximum amount of data that can arrive in a burst). Since an arriving packet to a FIFO queue has to wait for the backlog in the queue to be zero before it will be forwarded on the output link at rate Cout, Equation (14) becomes:

$$W_{Cout}\left(R\right)\left(t\right) = \max_{s \le t}\left[\int_{s}^{t} R_{in}(t)dt - C_{out}(t-s)\right] \qquad (15)$$

where, Wcout(R)(t) = backlog inside the queue and Rin(t) = rate function of the incoming traffic at time t. Putting (8) into (15), we have:

$$d_{j} = \frac{1}{C_{out}} \max_{s \le s_{j}}\left[\int_{s}^{s_{j}} R_{in}(t)\,dt - C_{out}(s_{j}-s)\right] \qquad (16)$$

Since our intention in this model is to provide a maximum bound on the queuing delay (that is, dj), how then do we determine the interval [s, sj] for which dj is maximum? This will have to correspond to the maximum burst traffic arrival period of the incoming traffic. But Cout is fixed, this is because, the FIFO queue is a degenerate FCFS MUX (Cruz, 1991), and we assume that the FCFS MUX is work-conserving; that is, if B(t) is the backlog at time t and B(t)>0 at any instant of time t, then, Rout(t) = Cout (Cruz, 1991). So definitely, the interval [s, sj] where dj is maximum only depends on the arrival process of the traffic Rin(t). This is illustrated in Figure 10. We now proceed to determine a possible traffic arrival interval where dj would be maximum by following the procedure developed by Georges et al., (2005). Recall that Rin is the rate function of the incoming traffic stream;

$$\forall\, s_{j} \ge s$$

$\int_{S}^{S_{j}} R_{in}(t)\,dt$ is the amount of traffic that have arrived in the closed interval [s, sj].

Given σ ≥ 0, and ρ ≥ 0, we write Rin ~ (σ, ρ), if and only if for all s, sj satisfying sj ≥ s, there holds:

$$\int_{S}^{S_{j}} R_{in}(t)dt \le \sigma + \rho\,(s_{j}-s) \qquad (17)$$

Similarly, if b is any function defined in the non-negative reals, and Rin ~ b, we can write (Georges et al., 2005; Cruz, 1991):

from literature. We now give a simple explanation of the validation that was carried out.

Assume we are dealing with a switched Ethernet LAN (which is almost the only type of switch LAN that is deployed by organizations). We use also, the maximum packet size of an Ethernet packet (the extended Ethernet packet), which is 1530 bytes (8-bytes preamble + 18-bytes header + 1500 data bytes + 4-bytes CRC). The maximum packet size is used, because, we are seeking to establish an upper bound delay, and hence, there is the need to maximally load the switch.

Assume also, that, $\sigma =$ Ethernet frames = 340 Ethernet frames. This is the average of IETF (Internet Engineering Task Force). RFC (Request for Comments) 2544 (see RFC 2544, (2009)) recommended values for Device under Test (DUT) to switching devices manufacturers. With these values of L (1530 bytes × 8 bits) and σ (340 × 1530 bytes × 8 bits) inserted into Equation (35) with appropriate C's and N, the maximum delay value of the model is 42 milliseconds (42 ms).

Georges et al. (2005) reported that the maximum delay value obtained with the maximum delay Ethernet packet switch model reported in the paper is $3080\,\mu s$ or $3.080\,ms$; while the COMNET 111 simulation software package gave a maximum delay value of 450 μs or 0.450 ms. Using 100 ms which is the upper delay bound for IEEE 802 networks as recommended in IETF's RFC 2815: Integrated Services Mappings on IEEE 802 Networks (see RFC 2815, (2009)), we make the following simple comparisons.

1. The maximum delay value obtained by Georges et al. (2005). This value is 3.080 ms. Using 100 ms end-to-end application delay bound, it will mean that between two hosts (one, the origin host and the other, the destination host) there can be $\frac{100\ ms}{3.080\ ms} = 32.5 \cong 33$ switches.
2. The maximum delay value provided by COMNET 111 as reported by Georges et al. (2005). This value is 0.450 ms. Using 100 ms end-to-end application delay bound, it will mean that between two hosts (one, the origin host and the other, the destination host) there can be $\frac{100\ ms}{0.450\ ms} = 222$ switches.
3. The maximum delay value provided by the model represented by Equation (35). This value is 42 ms. Using 100 ms end-to-end application delay bound, it will mean that between two hosts (one, the origin host and the other, the destination host) there can be $\frac{100\ ms}{42\ ms} = 2.4 \cong 3$ switches.

Square D's (2009) specifications for the installation of the Model SDM 5DE 100, Class 1400 Ethernet packet switch is: 'switches can be concatenated between devices (hosts) as long as the path between hosts does not exceed four (4) switches and five (5) cable runs.' From the information provided by this manufacturer, it can be seen that in practical terms, the model represented by Equation (35) is close to reality, unlike, the values provided by the models obtained from literature (and it is therefore, validated).

CONCLUSION

This work has highlighted the switched LANs' delay problem. It has also discussed briefly, the evolution of switched Ethernet LANs, and, has discussed the two principal approaches of determining the end-to-end delays of computer communication networks (the stochastic approach and the deterministic approach), bringing out the fact that the latter has obvious advantages over the former. The work then took a brief excursion in to

the deterministic approach, and demonstrated its application by using it to model a packet switch using the network components that were proposed and specified by Cruz (1991). The packet switch model was shown to be good for the practical engineering of local area networks that meets specified maximum end-to-end delay constraints.

FUTURE RESEARCH DIRECTIONS

Some problems' areas have been discovered in the course of our research work. The most pressing of these, is, the determination of a value for the maximum amount of traffic that can arrive to a network (or switch) in a burst. This parameter is termed σ in our chapter. This is presently an area of very intense research activity. In fact, it is the, believe here that, coming out with an empirically validated value for σ (or how to determine σ) will be a major breakthrough to the Internet and Networking research community.

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KEY TERMS AND DEFINITIONS

σ: The maximum amount of traffic that can arrive to a system in a burst.

ρ: The long-term average rate of traffic flow to a system.

~: Roughly similar, or poorly approximates.

ATM: Asynchronous Transfer Mode.

CSMA/CD: Carrier Sense Multiple Access with Collision Detection.

LAN: Local Area Network.

QoS: Quality of Service.