A model predictive control-based STATCOM for weak grid voltage enhancement

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H I G H L I G H T S

- Finite control set MPC was developed in the synchronous reference frame with a cost function for STATCOM control.
- The overall strategy uses outer loop PI controllers for STATCOM DC voltage and grid voltage magnitude control.
- Time delay compensation in transport, sampling, filtering, and ADC was considered in PI controller gains.
- A robust AHPF-DSOGI-based PLL was developed for STATCOM synchronization with a weak grid.
- The MPC with robust grid synchronization enabled the STATCOM to mitigate voltage swell, dip, and harmonics.

A R T I C L E   I N F O

A B S T R A C T

This paper presents a model predictive control (MPC) technique for the control of reactive power flow from a static synchronous compensator (STATCOM) into a weak power system network. The MPC strategy enables the STATCOM to mitigate weak phase voltage magnitudes in a distribution grid. The weak voltage magnitudes usually emanate from large inductive loads connected to the grid's point of common coupling (PCC). The MPC utilizes a finite control set of voltage vectors to minimize a cost function, which reduces the errors between set references and the corresponding predicted variables. The references in the cost function are set by two outer loop controllers. A time delay compensation strategy is introduced and proposed for selecting the gains of the outer loop controllers. An LC filter was also designed at the STATCOM's output terminals to confine the harmonics in the injected compensation current to permissible limits. A robust all high pass filter dual second order generalized integrator (AHPF-DSOGI) based phase locked loop (PLL) is developed and proposed for synchronization of the STATCOM into the weak grid. The overall MPC strategy on the STATCOM enables shunt injection of compensation currents at the PCC while mitigating harmonics and consequently improving power quality. The STATCOM effectively regulated the bus voltage when required by switching between the capacitive and inductive modes. Results showing the efficacy of integration of the STATCOM to the grid and robust capabilities of the STATCOM in mitigating voltage swell and dip, as well as harmonics, are presented.

1. Introduction

In recent times, there has been an increased awareness of problems associated with power quality by customers and power system operators, as this commonly affects them negatively. Consequences of power quality problems include economic losses, reduced efficiency of equipment, total loss of equipment, and voltage instability. Voltage instability is predominantly one of the most common power quality problems, and it exists in various forms, such as voltage sags, swells, and dips [1,2]. There is a direct correlation between voltage stability and reactive power. To maintain a steady magnitude of voltage profile, reactive power flow in a power system must be well managed [3]. Management in this context considers keeping the reactive power of a power system network within predefined limits. As such, reactive power compensation is sacrosanct for voltage stability in any power system network.

A static synchronous compensator (STATCOM) is a fast-acting shunt-connected flexible alternating current transmission system (FACTS) device applicable for reactive power compensation. The initial concept of STATCOM emanated as devices for reactive compensation in transmission networks, where voltage magnitude and frequency are maintained steady. However,

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in recent years, STATCOMs have been well applied in distribution grids with weak points of the common connection (PCC) voltage magnitudes. A typical STATCOM absorbs or injects reactive power into a grid depending on the state of the power system it is connected to [4]. STATCOM can also be considered a controllable current source that has three operating modes: idle, capacitive, and inductive mode [4,5]. The capacitive or inductive output current of the STATCOM can be controlled independently of the AC line voltage. When the system voltage is below the reference voltage (voltage sag), the STATCOM works in capacitive mode to restore the system voltage to its nominal value at the PCC. This is achieved by supplying reactive power to the grid through the PCC. Also, when voltage swells occur, the STATCOM works in inductive mode to restore the system voltage to its nominal value at the PCC by absorbing reactive power from the grid [6]. The dynamic response of a STATCOM is fast compared to other FACTS devices. STATCOM control techniques such as vector control, nonlinear hysteresis-based control such as sliding mode control, and model predictive control (MPC) were presented [7-9].

In the past, MPC was only dominant in process control applications such as chemical process control lines, etc., but lately, it is gaining wide interest for control of power electronics-based devices such as STATCOM [10-13]. A unique advantage of MPC is that nonlinearities and constraints associated with the controlled system can be easily taken into consideration during the design and implementation stages [12]. With the proliferation of fast processors in recent times, the real-time computation required in optimization procedures for MPC no longer poses a challenge. As such, the real-time computation for minimization of the cost function in MPC can be achieved in micro or even nanoseconds [11,12] Therefore, MPC is a viable and better alternative to conventional vector control schemes because it eliminates the challenges associated with tuning PI controllers for stability of inner-current loop regulation.

Moreover, MPC is less sensitive to system parameters mismatched like the vector control. In literature two major categories of MPC are available for control of power electronics devices, namely: Finite Control Set MPC (FCS - MPC) and Continuous Control Set MPC. The FCS-MPC technique has a finite set of switching states that are defined by the designer depending on the topology of the VSC scheme [10]. The switching state that best minimizes the objective function switches the STATCOM. Unlike the continuous set MPC, a modulator to switch the STATCOM will be required [10].

In this study, therefore, an FCS-MPC scheme is adopted for control of STATCOM having an LC filter for harmonic frequency mitigation at its output terminals. The FCS-MPC scheme is attractive due to its simplicity and robustness in control [14-19]. In the scheme, PWM modulators will not be required. The switching signals are determined from a set of voltage vectors that best minimizes a cost function obtained from errors between output current vectors from STATCOM and set reference values. Unlike in [14], which is a cascade-free MPC with all the controlled variables and their references in the cost function, herein only the q and d currents and their references are in the cost function, whereby the q and d current references in the cost function optimization are cascaded to the outputs of the voltage control loops based on proportional plus integral (PI) controllers. Consequently, unique methods of obtaining the gains of the PI controllers, including compensations of the transport, analog-to-digital converter, and processing delays emanating from the digital implementation of the overall control scheme, are developed [20-22].

Furthermore, integration of a STATCOM into a distribution grid with a weak point of common coupling will require a phase-locked loop (PLL) that is robust enough to accurately read the grid's frequency and other parameters despite distortions existing in the grid. A weak point of common coupling could have unbalanced magnitudes of phase voltages and phase bumps, and the frequency deviation may be significant. Moreover, harmonic contents in the grid may also be significant, and the voltage sensors used in measuring the grid's line voltages may have some DC offsets in their readings. Therefore, the capability of the basic synchronous reference frame PLL (SRF-PLL) [23] for accurately reading the grid's frequency, phase angle, phase sequence, and voltage magnitude may be significantly degraded. Consequently, different configurations of the dual second-order generalized integrator (DSOGI) have been suggested in the literature for grid integration of inverter-based energy resources [24-27]. Bandpass filters and low pass filters were used originally in developing the conventional DSOGI, but the problem encountered then was the inability of the low pass filter to block DC offset because it has no zero at the origin. On the other hand, the bandpass filter will block the DC offset because it has a zero at the origin.

Consequently, the cited references on DSOGI herein developed different strategies for enhancing the low pass filters in DSOGI to block DC offsets. However, methods of cascading the low pass filter arms to the outputs of the bandpass filter arms were not critically assessed for DC blocking enhancement. Therefore, such unique cascades are investigated in this article with a view to developing new enhancement strategies for the DSOGI. Hence, a new DSOGI is developed from second-order high-pass filters that are different from the ones in [24-27] and introduced for synchronizing the SATCOM to a weak grid.

2. System configuration

The system is configured, as shown in Figure 1, with the inverter in the STATCOM as a 2-level voltage source inverter (VSI). It consists of a DC capacitor (Cdc), voltage source converter, and LC filter connected to the grid via a step-up transformer. The control laws are generated based on the reactive power requirements at the PCC.

Six IGBTS with free wheeling diodes across are connected, as shown in Figure 1, to form the voltage source inverter. When the PCC voltage is greater than the reference voltage, the STATCOM absorbs reactive power from the grid. Likewise, if the voltage at the PCC is less than the reference voltage, the STATCOM supplies reactive power to enhance the PCC voltage. The DC capacitor connected to the VSI ensures that reactive power is exchanged between the grid and the system. The LC filter eliminates the switching frequency harmonics, the L and C parameters are tuned to limit the harmonics within limits defined by [28].
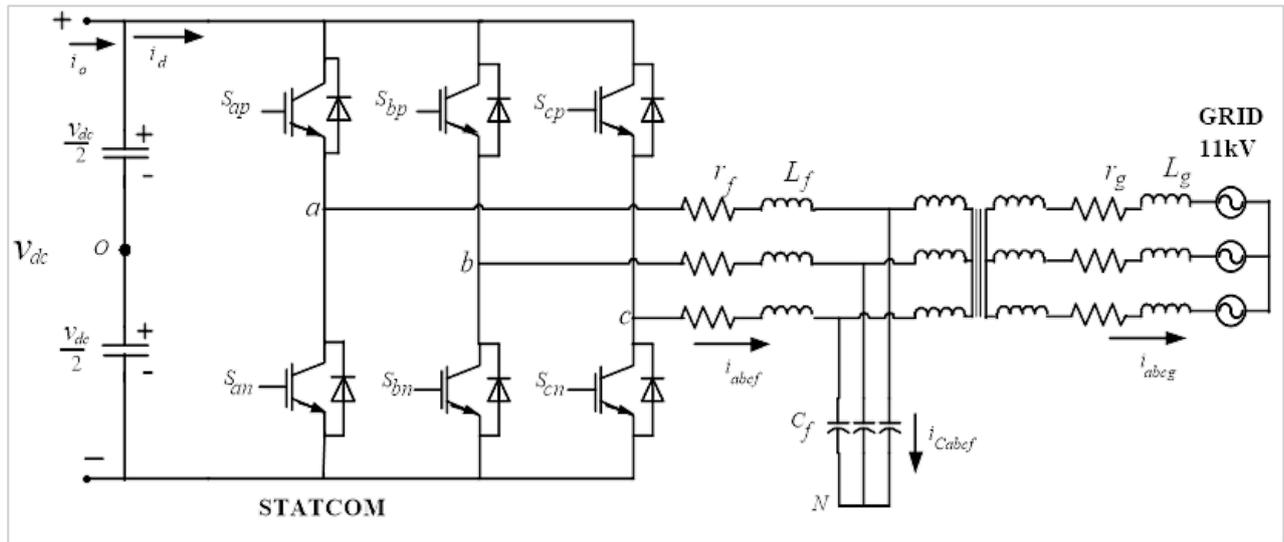
Figure 1: System Configuration

2.1 System model

By Kirchhoff's voltage law (KVL) and current law (KCL), the model equations of the STATCOM in Figure 1 were obtained in a natural 'abc' reference frame when rf is considered to be relatively small, as given in Equations (1) and (2):

$$v_{iabc} = L_f \frac{di_{abc}}{dt} + v_{g_{abc}} \tag{1}$$

$$i_{abc} = C_f \frac{dv_{fabc}}{dt} + i_{g_{abc}} \tag{2}$$

$$v_{fabc} \cong v_{g_{abc}} \tag{3}$$

In (2) and (3), $v_{f_{abc}}$ is the capacitor voltage, which is connected in a shunt with the grid's voltage $v_{g_{abc}}$. Assuming the filter capacitance is very small, the inverter current, i_{fabc} will be approximately equal to the grid current, $i_{g_{abc}}$. Therefore, the LC filter can be modeled as an L filter. Equations (1) and (2) in compact forms are expanded and transformed to the synchronous q d reference frame to achieve decoupled control of real and reactive power components. Consequently, the dynamic synchronous q d reference frame equations of the system are shown in (4) to (7). In state space, (4) to (7) transition to (8) to (11) respectively.

$$v_q = L_f \frac{di_q}{dt} + V_{g_q} + \omega L_f i_d \tag{4}$$

$$v_d = L_f \frac{di_d}{dt} + V_{g_d} - \omega L_f i_q \tag{5}$$

$$i_{qf} = C_f \frac{dv_{gq}}{dt} + \omega C_f v_{gd} + i_{qg} \tag{6}$$

$$i_d = C_f \frac{dv_{gd}}{dt} - \omega C_f v_{gq} + i_{dg} \tag{7}$$

$$\frac{di_q}{dt} = (v_q - V_{g_q} - \omega L_f i_d)\frac{1}{L_f} \tag{8}$$

$$\frac{di_d}{dt} = (v_d - V_{g_d} + \omega L_f i_q)\frac{1}{L_f} \tag{9}$$

$$\frac{dv_{gq}}{dt} = (i_q - \omega C_f v_{gd} - i_{qg})\frac{1}{C_f} \tag{10}$$

$$\frac{dv_{gd}}{dt} = (i_d + \omega C_f v_{gq} - i_{dg})\frac{1}{C_f} \tag{11}$$

2.2 Inverter model

The model output voltage equations of the two-level, three-phase voltage source inverter, in terms of switching functions used in implementing the STATCOM, are given in (12) to (14). The switching functions are represented by Sij where i= a,b,c (representing phases) and j = p,n (representing positive or negative switching), which takes a logic '1' when the semiconductor device it represents is switched on and the logic '0' when switched off. In an attempt to preserve KVL across the inverter, the top and bottom switches (IGBTs) of the same phase (leg) must not turn on at the same time, which means that the bottom switch complements the top switch. Therefore, in phase A leg for example, Sap + San = 1 for KVL to be fulfilled across phase A leg, which applies to phases B (Sbp + Sbn = 1) and C (Scp + Scn = 1). Consequently, knowing the switching function status of the top switches will be sufficient to determine the output phase voltages of the inverter given in (12) to (14). Hence, the three top switching functions will only give 8 states from a binary combination (23=8). The 8 switching states define the finite control set (FCS) used in the model predictive control (MPC) in the next Section. In many instances, MPC has been realized in the stationary q-d reference frame. Herein, however, the MPC is realized in the synchronous q-d reference frame because of the proportional plus integral (PI) controller that is used to control the STATCOM's DC-link voltage in a linear controller. As such, transforming (12) through (14) to the synchronous q-d reference frame yields (15) in compact form, where Ks is given in (16) while $V_{qd0} = [V_q \quad V_d \quad V_0]^T$ and $V_{abcn} = [V_{an} \quad V_{bn} \quad V_{cn}]^T$. In complex form $V_{qd} = V_q + jV_d$.

$$V_{an} = \frac{V_{dc}}{3}\left(2S_{ap} - S_{bp} - S_{cp}\right) \tag{12}$$

$$V_{bn} = \frac{V_{dc}}{3}\left(2s_{bp} - S_{ap} - S_{cp}\right) \tag{13}$$

$$V_{cn} = \frac{V_{dc}}{3}\left(2s_{cp} - S_{bp} - S_{ap}\right) \tag{14}$$

$$V_{dq0} = K_s V_{abcn} \tag{15}$$

$$K_s = \frac{2}{3}\begin{bmatrix} \cos(\theta_e) & \cos(\theta_e - \frac{2}{3}\pi) & \cos(\theta_e + \frac{2}{3}\pi) \\ \sin(\theta_e) & \sin(\theta_e - \frac{2}{3}\pi) & \sin(\theta_e + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{16}$$

3. Model predictive control as inner loop control

The MPC predicts the future state of the controlled variables utilizing the model of the system under consideration scheme [10]. The performance of a typical FCS-MPC controller is directly tied to the degree of accuracy of the system's model. In this case, the switching signals can be generated directly from the model of the system scheme [10],[13]. A cost (objective) function must be defined in MPC, which must be minimized by the selection of an optimal switching state that corresponds to the least cost function. Since a 2-level inverter is used, the selection of the optimal switching state is confined to the 8 switching states.

To apply model predictive control to the system, the dynamic equations of the system shown in Figure 2 were discretized using Euler's forward method given in (17) as applied in Singh et al. (2009). Therefore, applying equations (17) to (8) to (11) yields (18) and (21).

$$\frac{dx}{dt} = \frac{x_{(k+1)} - x_k}{T_s} \tag{17}$$

$$i_{q(k+1)} = i_{q(k)} + \frac{T_s}{L_f}(v_{q(k)} - v_{gq(k)} - \omega L_f i_{d(k)}) \tag{18}$$

$$i_{d(k+1)} = i_{d(k)} + \frac{T_s}{L_f}(v_{d(k)} - v_{gd(k)} + \omega L_f i_{q(k)}) \tag{19}$$

$$v_{gq(k+1)} = v_{gq(k)} + \frac{T_s}{C_f}(i_{qf(k)} - \omega C_f v_{gd(k)} - i_{qgf(k)}) \tag{20}$$

$$v_{gd(k+1)} = v_{gd(k)} + \frac{T_s}{C_f}(i_{df(k)} + \omega C_f v_{gq(k)} - i_{dgf(k)}) \tag{21}$$

The prime objective of STATCOM is to inject or absorb the required current into or from the grid to deliver the defined magnitude of active and reactive power. To achieve this, a cost function g is defined in (22). This cost function will evaluate and enable the selection of the switching state that minimizes it.

$$g = W_1 \left| i_d^* - i_{d_{(k+1)}} \right| + W_2 \left| i_q^* - i_{q_{(k+1)}} \right| \tag{22}$$

In (22), i_d^* and i_q^* are the reference control vectors. The control variables do not contribute equally to the cost function due to the difference in their nature. To enhance the optimal selection of the switching states and tracking of reference signals, weights are attached to the terms in the cost function [10]. The weighting factors values have a direct influence on the system's performance, however, there is yet to be a well-defined procedure for weight selection. The branch and bound technique, as described by [10], was used in weight selection.
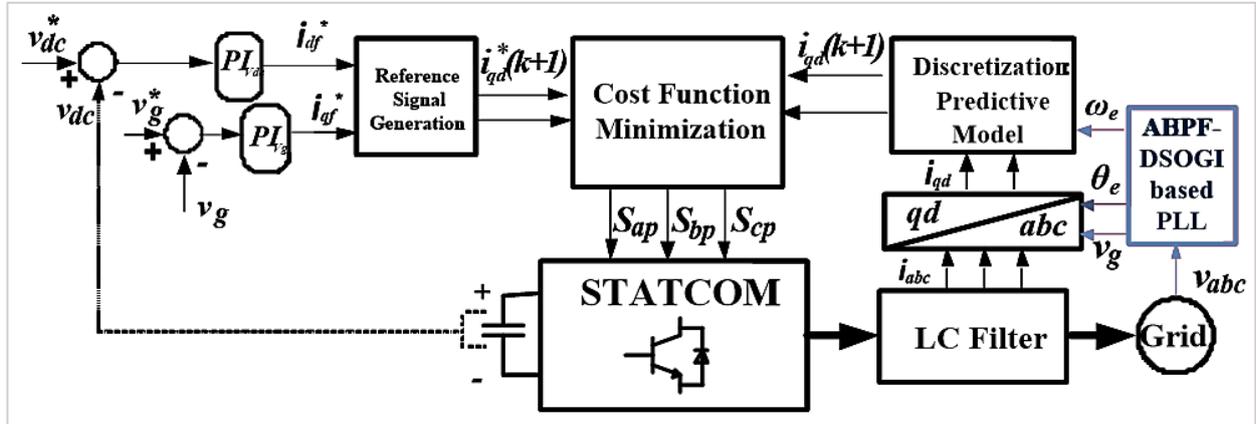
Figure 2: Schematic of the Control System

4. Outer loop control

In making the STATCOM respond dynamically to disturbances at the PCC, two proportional plus integral (PI) controllers were used in outer loop control to generate the q and d current references required by the cost function in the inner current model predictive controller. Therefore, the grid's voltage was aligned along the d-axis to have a decoupled control whereby the DC capacitor's voltage is controlled along the d-axis, and the grid's voltage magnitude is controlled along the q-axis. Consequently, the references i_d^* and i_q^* in the cost function of (22) were synthesized from the outputs of the outer loops DC capacitor voltage control and grid's voltage magnitude control respectively, which are given subsequently.

4.1 DC Capacitor voltage control

In designing the DC capacitor voltage controller, the inverter's DC input power was balanced with the real part of the inverter's AC output power, as shown in (23). The real power balance was possible because the grid's voltage was aligned along the d-axis, which yields $V_{gd} = V_g$ and $V_{gq} = 0$, where $V_{gd}^2 + V_{gq}^2 = V_g^2$. In the capacitor, the DC drawn is relative to its capacitance and rate of change of its voltage with time, as shown in the equation (24). Substituting (24) in (23) yields (25). Resolving (25) establishes the i_d^* reference for the cost function in (22) for the inner current MPC. δ_{vdc} in (25) and (26) defines the closed loop capacitor voltage control, whereby kdc is the PI controller. In the (27), which defines kdc in terms of the proportional (k_p) and integral (k_i) gains, $\tau_i = k_p/k_i$. The k_p and k_i for the controller in (27) must be selected to guarantee a stable operation of the outer loop control. Equation (29) gives the reference i_d^* current required by the MPC to resolve the cost function shown in (22).

$$I_{dc}v_{dc} = \frac{3}{2}v_d i_d \tag{23}$$

$$C_{dc}\frac{dv_{dc}}{dt} = I_{dc} \tag{24}$$

$$C_{dc}\frac{dv_{dc}}{dt} = \frac{3v_d i_d^*}{2\,v_{dc}} = \delta_{vdc} \tag{25}$$

$$\delta_{vdc} = k_{dc}(v_{dc}^* - v_{dc}) \tag{26}$$

$$k_{dc} = k_p + \frac{k_i}{s} = k_p\left(\frac{s+1/\tau_i}{s}\right) \tag{27}$$

$$\delta_{vdc} = \frac{3v_d i_d^*}{2\,v_{dc}} \tag{28}$$

$$i_d^* = \frac{\delta_{vdc}}{\frac{3v_d}{2\,V_{dc}}} \tag{29}$$

In selecting the gains of k_{dc} the open loop and closed loop transfer functions of the DC capacitor voltage control in (25) and (26) can be obtained as given in (30) and (31), respectively. In digital control of the STATCOM, there exists a cumulative delay, T_d, which combines the time delays from transport, sampling, filter processing, analog-to-digital converter (ADC), etc. As such a delay compensator $H_d(s) = e^{-sT_d}$ was introduced to (30) as given in (32). $H_d(s)$ in (32) was approximated by an all-pole approximation of its Taylor time series. Therefore, $H_d(s) = e^{-sT_d} \approx 1/(sT_d + 1)$ [20-22] is the first-order approximation. Consequently, the closed loop transfer function in (33) was obtained, which gives the gain parameters when the denominator in (33) is compared to 3rd order Butterworth polynomial given as $(s + \omega_n)(s^2 + s\omega_n + \omega_n^2)$. Equation (34) was obtained in terms of Td, which invariably defines the gains in (35) and (36) in terms of Td. The root loci plot for (33) is shown in Figure 3.

$$H_{o\_dc}(s) = \frac{v_{dc}(s)}{v_{dc}^*(s) - v_{dc}(s)} = \frac{v_{dc}(s)}{e(s)} = \frac{k_{dc}}{sC_{dc}} = \frac{k_p(s + 1/\tau_i)/C_{dc}}{s^2} \tag{30}$$

$$H_{c\_dc}(s) = \frac{v_{dc}(s)}{v_{dc}^*(s)} = \frac{k_{dc}(s)/C_{dc}}{s + k_{dc}(s)/C_{dc}} \tag{31}$$

$$H_{o\_dc}(s)H_d(s) = \frac{k_{dc}(s + 1/\tau_i)/C_{dc}}{s^2} \cdot e^{-sT_d} \approx \frac{k_{dc}(s + 1/\tau_i)/C_{dc}}{s^2} \cdot \frac{1}{sT_d + 1} \tag{32}$$

$$H_{cd\_dc}(s) = \frac{\frac{k_p}{C_{dc}T_d}s + \frac{k_p}{\tau_i C_{dc}T_d}}{s^3 + \frac{s^2}{T_d} + \frac{k_p}{C_{dc}T_d}s + \frac{k_p}{\tau_i C_{dc}T_d}} \tag{33}$$

$$\omega_n = \frac{1}{2T_d} \tag{34}$$

$$k_p = \frac{2\omega_n^2 C_{dc}T_d}{2} = \frac{C_{dc}}{2T_d} \tag{35}$$
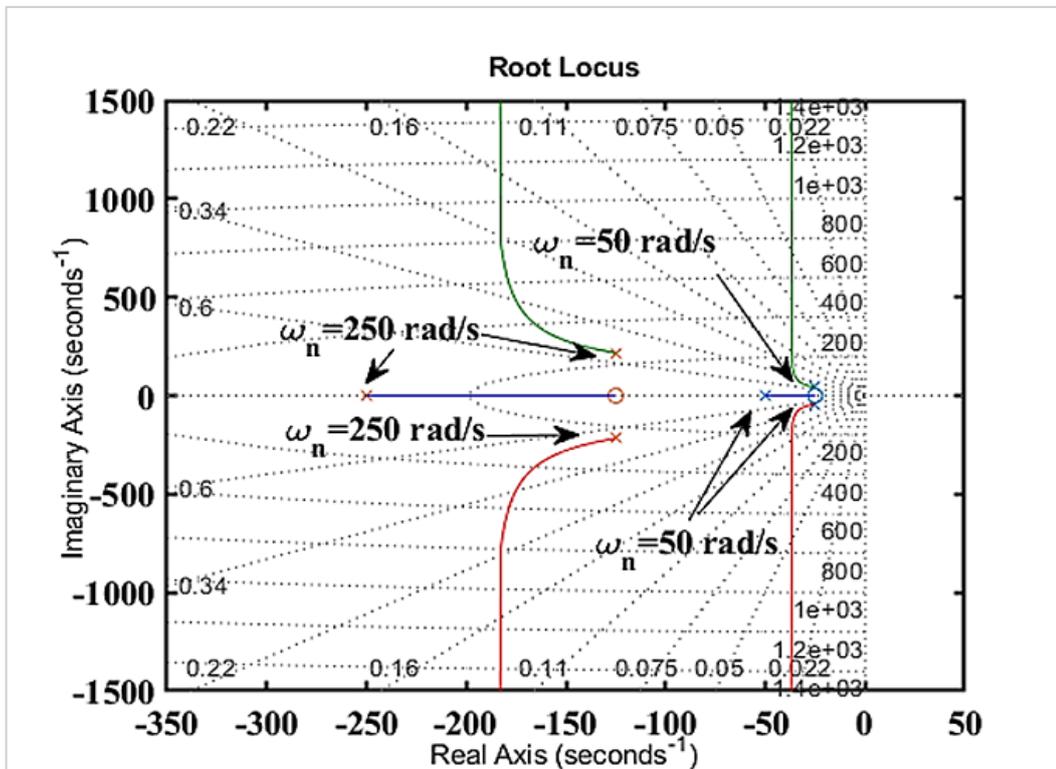
$$\tau_i = \frac{2}{\omega_n} \tag{36}$$

Figure 3: Root Locus

5. Grid's voltage magnitude control

Expanding equation (2) and transforming to the synchronous q-d reference frame yields equations (37) and (38). Therefore, (37) yields (39) and is used to obtain the grid's voltage magnitude control given in (40). The PI control k_{Vg} is defined in (41). Consequently, the reference for the q-axis current in the cost function of (22) is given in (42).

Following through the derivation of (33), the transfer function of (43) is derived. Therefore, the selection of gain parameters in (43) is similar to those in (34) to (36) in terms of T_d. Therefore, the same stability conditions that apply to (33) apply to (43).

$$C_f \frac{dV_{g_q}}{dt} + \omega V_{g_d} C_f = i_q - i_{g_q} \tag{37}$$

$$C_f \frac{dV_{g_d}}{dt} - \omega V_{g_q} C_f = i_d - i_{g_d} \tag{38}$$

$$C_f \frac{dV_{g_q}}{dt} = i_q^* - i_{g_q} + \omega V_{g_q} C_f = \boldsymbol{\delta}_{Vg} \tag{39}$$

$$\boldsymbol{\delta}_{Vg} = k_{Vg}\left(V_g^* - V_g\right) \tag{40}$$

$$k_{Vg} = k_{pg} + \frac{k_{ig}}{s} = k_{pg}\left(\frac{s + 1/\tau_{ig}}{s}\right) \tag{41}$$

$$i_q^* = \boldsymbol{\delta}_{Vg} + i_{g_q} - \omega V_{g_q} C_f \tag{42}$$

$$H_{cd\_g}(s) = \frac{\frac{k_{pg}}{C_f T_d}s + \frac{k_{pg}}{\tau_{ig} C_f T_d}}{s^3 + \frac{s^2}{T_d} + \frac{k_{pg}}{C_f T_d}s + \frac{k_{pg}}{\tau_{ig} C_f T_d}} \tag{43}$$

6. Parameter selection

6.1 The capacitance of the DC input capacitor

This is the source of DC input voltage for the VSI, and its value is based on the capacity of the STATCOM, DC link voltage, and expected time of action to mitigate voltage sags and swells at the PCC [4].

It should be noted that during the compensation action of the STATCOM to restore the PCC voltage to its desired value, there will be variations in the DC link voltage. In selecting a suitable capacitor, a suitable tolerance that will accommodate the deviation of the DC Link voltage from the reference during STATCOM action should be defined. In this paper, a deviation of ±5% of the DC link voltage action time of one period was used in selecting the required capacitance that will provide the needed energy. The reference DC link voltage is given in (44), where Vm is the peak phase voltage of the low voltage side of the transformer. In (45), the DC input capacitance is obtained.

$$Vdc_{ref} = 3Vm \tag{44}$$

$$Cdc = \frac{2Q_s p}{f_o(Vdc_{ref}^2 - Vdc_{refmin}^2)} \tag{45}$$

where Q_s is = 1 MVAR, p is the period = 1, f_o= 50 Hz, Vdc_{ref} = 6000 V, Vdc_{refmin} = 0.9Vdc_{ref}

6.2 LC Filter

The LC filter should have the capacity to attenuate high-frequency switching harmonics while maintaining a low voltage drop at the system's fundamental frequency and having a negligible effect on the reactive power compensation ability of the STATCOM [30]. Several techniques have been proposed for the selection of the filter inductance by [30-32]. The FCS-MPC control strategy implemented in this paper has a variable switching frequency. In this design, the filter inductance was limited to 0.1pu. In (46), I_n is the maximum current the system can handle, and f_o is the frequency of the system.

$$l_f = \frac{0.1 V_m}{2\pi f_o I_n} \tag{46}$$

According to [31], for good performance of the STATCOM, the capacitance has to be as small as possible so as to minimize the fundamental current that will flow through it at rated capacity. The capacitance of the filter was limited to 5% of the base capacitance of the system, which is given in (47).

$$C_f = \frac{0.05 I_n}{2\pi f_n V_m} \tag{47}$$

7. AHPF-DSOGI for grid synchronization of STATCOM

Integration of the MPC-based STATCOM into the weak grid could pose some synchronization challenges if the grid's parameters, such as frequency, phase sequence, phase angle, and voltage magnitude, are not well detected. The phase voltages are usually typically not equal in weak grids, and once there exist such unbalanced phase voltages, the q-d synchronous reference frame transformation required by the phase-locked loop (PLL) generates second harmonics in the synchronous q-axis and d-axis grid's voltages. Moreover, some slight DC offsets may exist in phase voltages of weak grids, or the DC offsets may emanate from the voltage sensors required for detecting the grid's parameters. A basic PLL for grid synchronization is the synchronous reference frame PLL (SRF-PLL) [23], and it consists of a phase detector (PD), a voltage control oscillator (VCO), and a loop filter (LP). The SRF-PLL, if not enhanced, is not robust enough to ride through the weak grid's inadequacies. Consequently, with such SRf-PLL, a smooth grid synchronization of the STATCOM becomes impossible.

A conventional synchronization method to ride through deficiencies in weak grids presented in literature entails the introduction of the dual second-order generalized integrator (DSOGI) as a pre-filter into the PD of SRF-PLL [24-27],[29]. The conventional DSOGI is capable of separating the positive sequence from the negative sequence components, as depicted in Figures 4 (a) and (b). However, the conventional DSOGI in Figure 4 is deficient because the low pass filter (LPP) arms cannot block DC offset because they do not have zeros at the origin. On the other hand, the band pass filter (BPF) arms can block DC offset because they have a zero at the origin. Hence, other configurations have been proposed to enhance the DSOGI [24-27],[29]. In this article, however, an all high pass filter DSOGI (AHPF-DSOGI) is introduced for synchronization of the MPC based STATCOM into a weak grid. Second-order HPF is used for the AHPF-DSOGI herein. Second-order HPF has two zeroes at the origin, which makes it capable of blocking DC offset, as can be seen in the Bode plot of Figure 5. The AHPH-DSOGI in this article is different from the multi-second order SOGI (multi SO SOGI) presented in Xin et al. [27], that is depicted in Figure 6, which used LPFs and BPFs because only second order high pass filters are used as depicted in Figure 7. Moreover, figure 6 will require more filters than Figure 7. Furthermore, the compensation strategy embedded in gain magnitude and phase offset is different from that of [27]. In [27], Laplace transformations were used for realizing the compensators for phase margins, while the AHPF-DSOGI herein uses exponential functions at the output of the filter cascades as correctors to remove and correct phase offsets from the filters.

The gain magnitude and phase offset of the second-order HPF are given in (48). Therefore, the correctors for the magnitude and phase offset of the AHPF-DSOGI are obtained from (49) and (50), respectively. In (49) $|M|$ represents the magnitude in (48) $\emptyset$ and represents the phase offset of (48), while δ stands for the processing delay emanating from the digital implementation of the filter. Consequently, the corrector's output for the HPF is given in complex form in (51), which is expanded to $\alpha\beta$ components of (52) and (53). The corrector's output for the HPF*HPF cascade is given in the complex form in (54), which is expanded to $\alpha\beta$ components of (55) and (56). The overall AHPF-DSOGI-based PLL is depicted in Figure 8.

$$|H(j\omega_1)| = \frac{|k\omega_1^2|}{\sqrt{\left(\omega^2 - \omega_1^2\right)^2 + (k\omega\omega_1)^2}} \angle tan^- \left(\frac{k\omega\omega_1}{\omega^2 - \omega_1^2}\right) \tag{48}$$

$$G = \frac{1}{|M|} \tag{49}$$

$$P = e^{-j(\emptyset + \delta)} \tag{50}$$

$$v_{\alpha\beta}^c = G_H v_{\alpha\beta}' P_H \tag{51}$$

$$v_\alpha^c = G_H\left(v_\alpha' cos\emptyset_{H_1} + v_\beta' sin\emptyset_{H_1}\right) \tag{52}$$

$$v_\beta^c = G_H\left(v_\beta' cos\emptyset_{H_1} - v_\alpha' sin\emptyset_{H_1}\right) \tag{53}$$

$$v_{\alpha\beta}^c = G_{HH} v_{\alpha\beta}' P_{HH_1} = G_{HH}\left(v_\alpha' + jv_\beta'\right)e^{-j\left(\emptyset_{HH_1}\right)} \tag{54}$$

$$v_\alpha^c = G_{HH}\left(v_\alpha' cos\emptyset_{HH} + v_\beta' sin\emptyset_{HH}\right) \tag{55}$$

$$v_\beta^c = G_{HH}\left(v_\beta' cos\emptyset_{HH} - v_\alpha' sin\emptyset_{HH}\right) \tag{56}$$
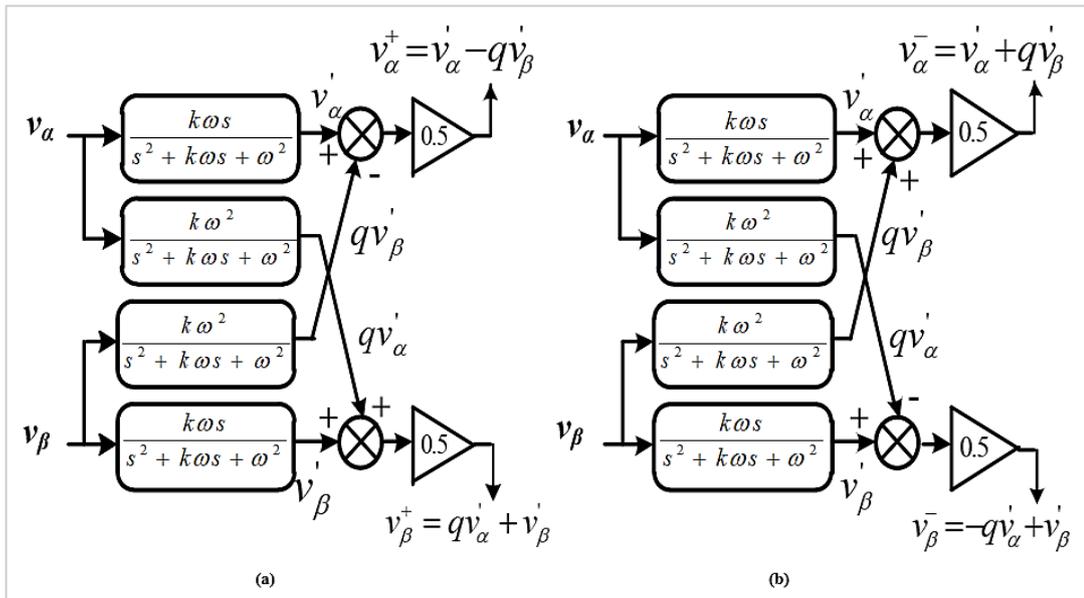
Figure 4: DSOGI (a) Positive sequence (b) negative sequence detectors
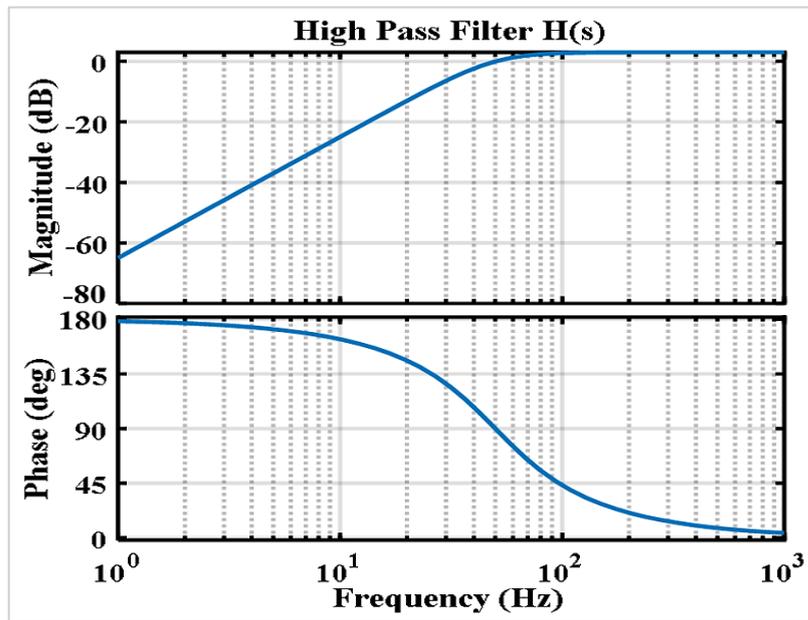

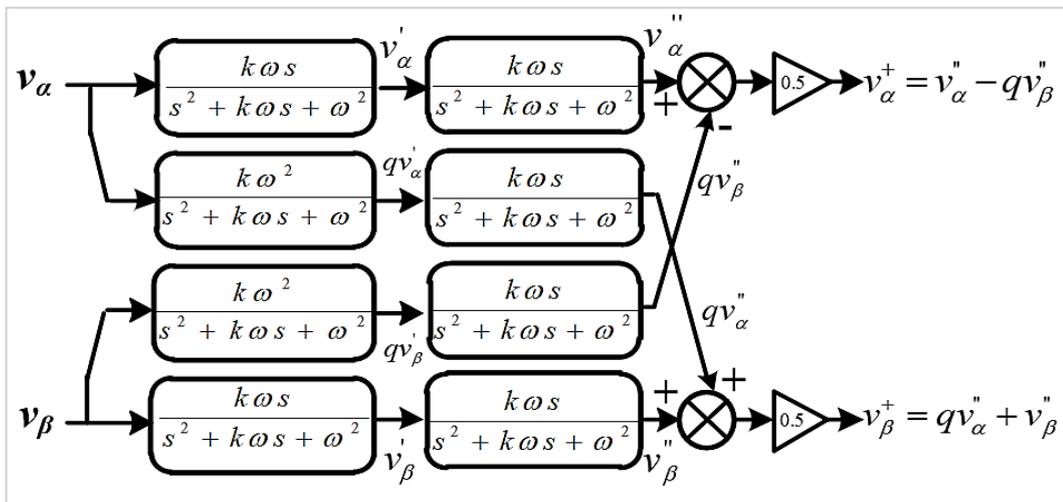**Figure 5:** Bode plot of second-order HPF

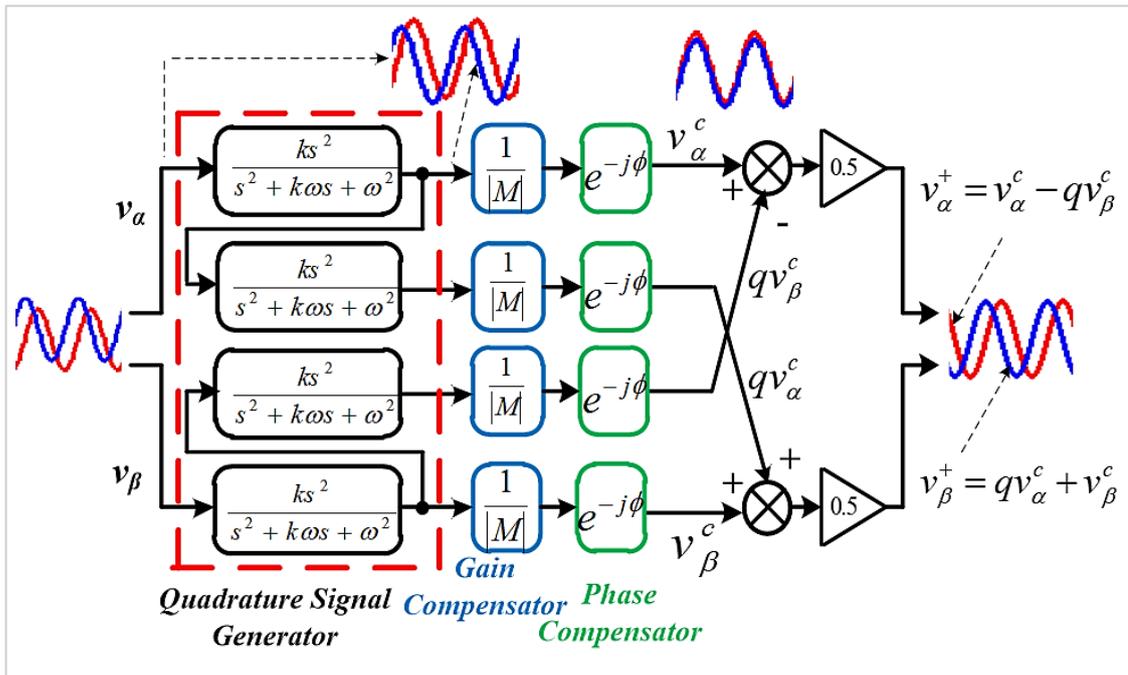
Figure 6: Second-order dual SOGI (SO DSOGI))

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Figure 7: Implementation of positive sequence detector embedded with compensators in AHPF-DSOGI
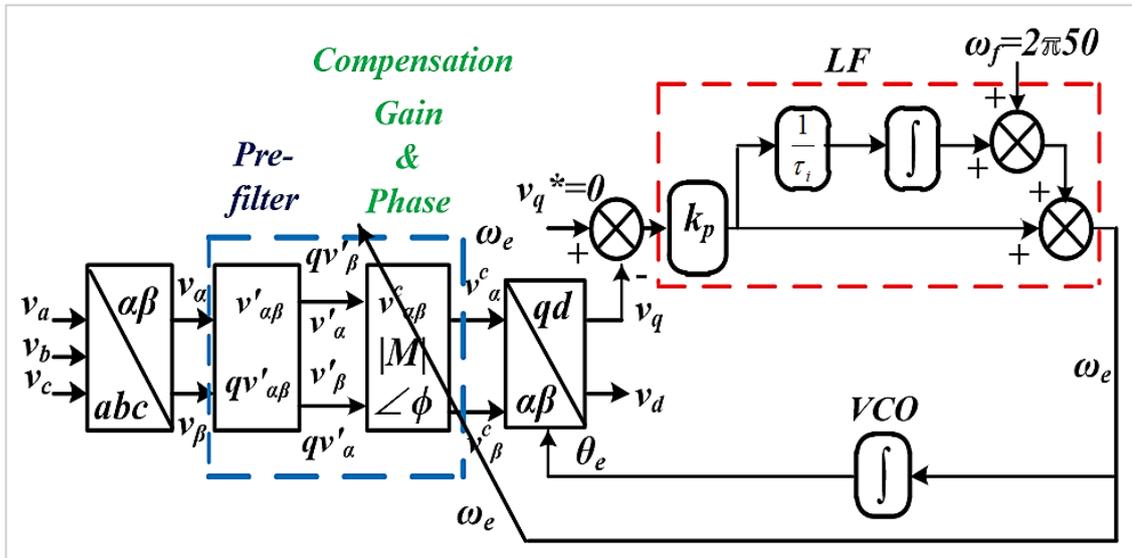

Figure 8: Proposed PLL configuration with PI as LF

8. Results and discussion

Simulation of the grid-connected STATCOM was done in MATLAB/SIMULINK environment. Parameters for simulation are given in Table 1. The simulation commenced by testing the AHPF-DSOGI-based PLL in a grid with unbalanced line voltages, while the voltage sensors used in measuring the grid's line voltages have some DC offsets. The efficacy of the AHPF-DSOGI was tested by introducing a frequency step change in the grid from 50 Hz to 51.32 Hz in 1.6 s to 4 s. The response of the AHPF-DSOGI-based PLL to the frequency step change was compared to the response of an improved discrete 3-phase PLL block in SIMULINK with the capability for harmonics and DC offset ride-through. The phase voltages obtained from the voltage sensors measured line voltages when scaled to a magnitude of 1 V are shown in Figure 9, with DC offsets. In Figure 10, the response to the frequency step change by a basic synchronous reference frame PLL (SRF-PLL) without any pre-filter (such as conventional DSOGI or AHPF-DSOGI) for synchronizing the STATCOM to the grid is shown and is seen to be heavily degraded by ripples. However, in Figure 11, the response of the AHPF-DSOGI-based PLL to frequency step change is shown and compared to the response from the improved discrete 3-phase PLL block in SIMULINK. It is seen in Figure 11 that the AHPF-DSOGI-based PLL has a lower offshoot after the step change. Moreover, the ripples seen in Figure 10 from the SRF-PLL have been completely mitigated in Figure 11.

Table 1: Parameters for Simulation

System Parameters	Values
DC Link Voltage	6000 V
DC Link Capacitance	8 mF
Filter Inductance	1.5 mH
Filter Capacitance	50 μF
Transformer	2.2 kV/11kV
Line Parameters	0.789 Ω / 46.58 mH
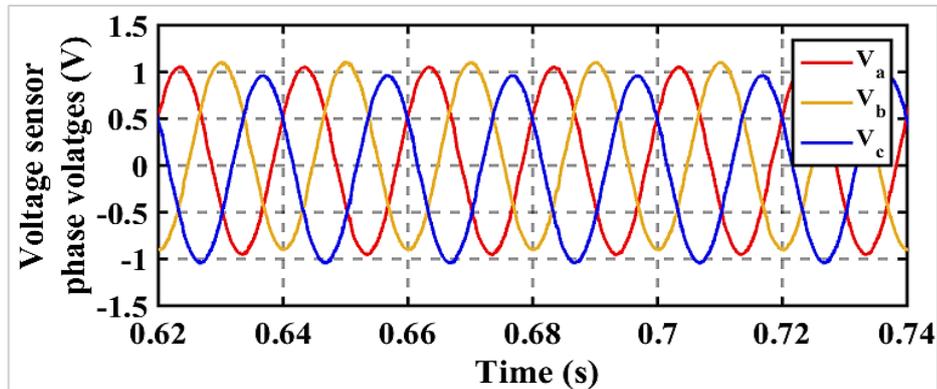
Figure 9: Phase voltages from voltage sensors with DC offsets
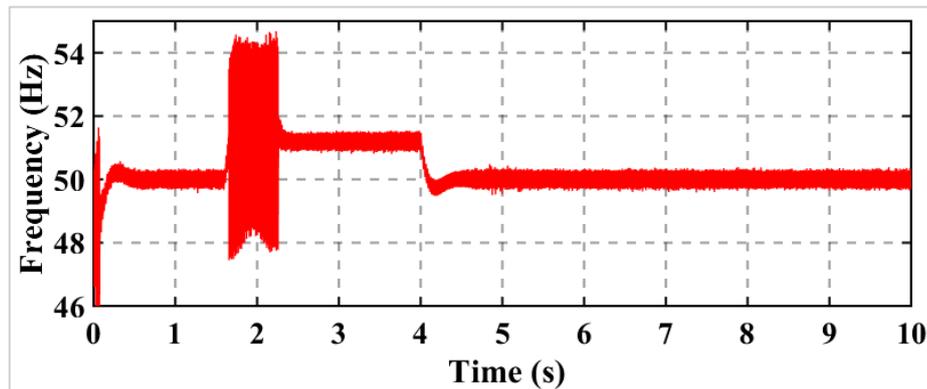
Figure 10: Frequency step change from SRF-PLL
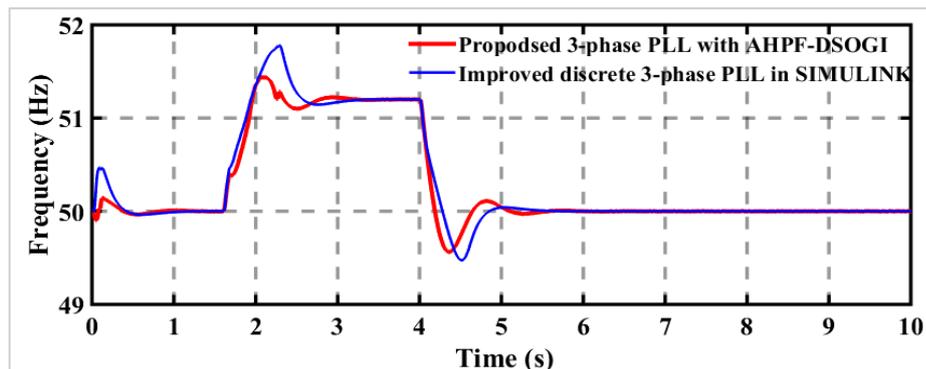
Figure 11: Frequency step change: Proposed AHPF-DSOGI-based PLL and improved discrete 3-phase PLL in SIMULINK

Furthermore in the simulation, the robustness of the STATCOM with its controller was tested by injecting sag and swell into the grid over a period. The nominal voltage of the test grid was 11 kV RMS (~ 15.6 kV Peak). At the PCC, the voltage at the start of the simulation was 9.9 kV (~14 kV peak), as shown in Figure 12. The voltage drop at the PCC can be attributed to the transmission line impedance and inductive loads connected at the receiving end of the grid. The voltage sag experienced by the grid was sustained till 0.6s, after which the grid experienced a voltage swell that resulted in an increase of the nominal

voltage at the receiving bus to 12.5 kV (~18 kV peak). At the 1s mark, the test grid attained its previous state before the voltage swell. Figure 13 presents a zoomed shot of Figure 12.
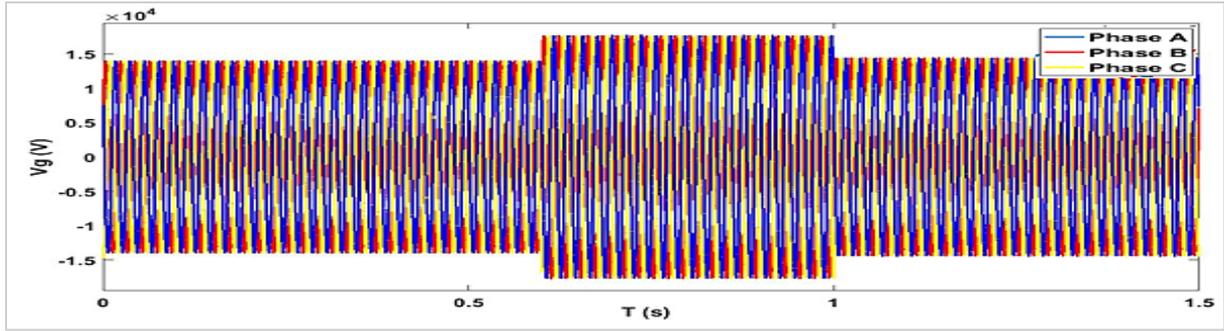

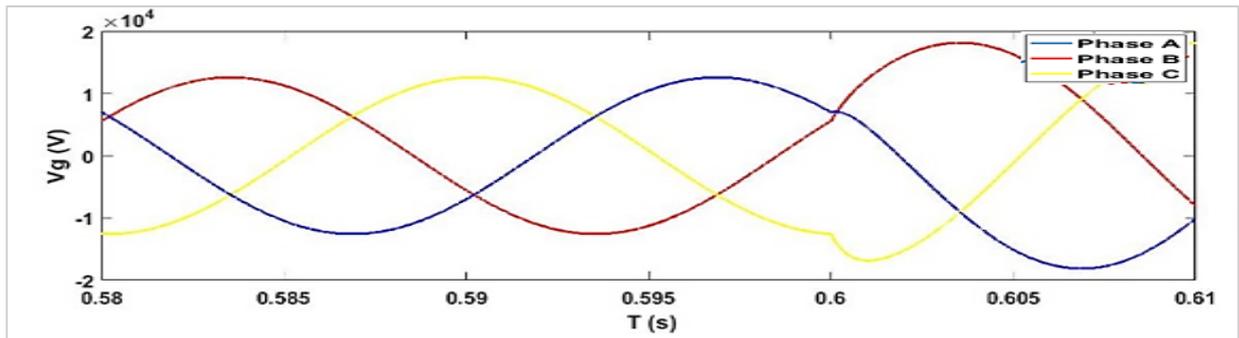**Figure 12:** Uncompensated Test Grid

Figure 13: Uncompensated Grid Experiencing a Sustained Under voltage and a Sudden Voltage Swell at the PCC

To mitigate this, the modeled STATCOM was connected to the test grid at the start of the simulation (0 s). Since the STATCOM had to act as soon as it was connected, voltage transients, which died out within 0.13s, were shown in Figure 14. The STATCOM successfully restored the bus voltage to the nominal value of 11 kV in less than a cycle. A zoomed shot of Figure 14 is presented in Figure 15.
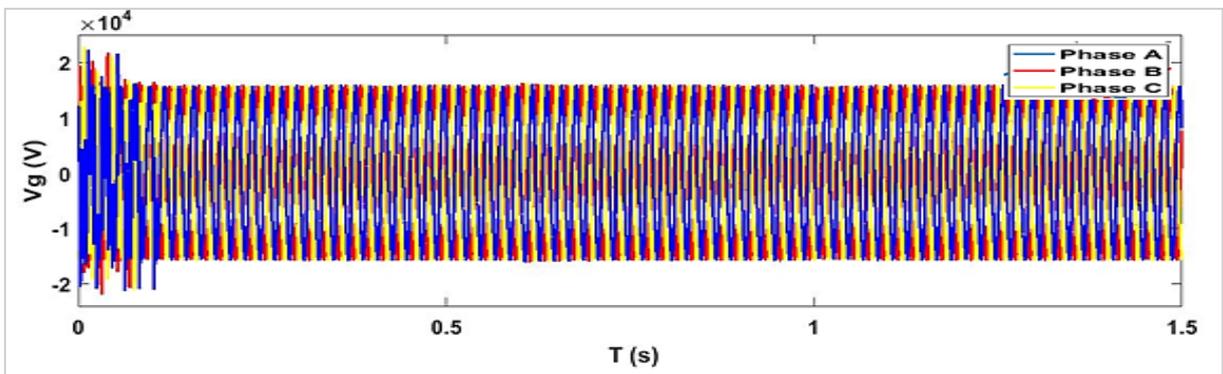

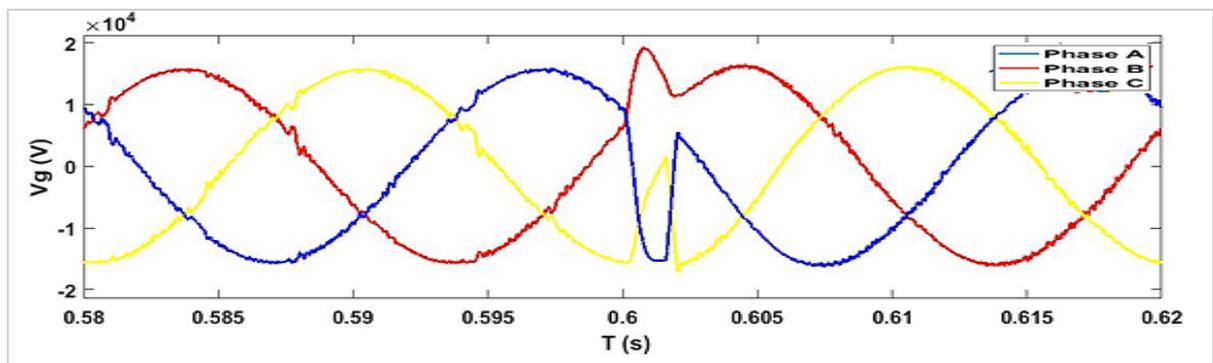**Figure 14:** Compensated Test Grid

Figure 15: Compensated Grid Acted on by the STATCOM to Restore the Bus Voltage to 15.6 kV Peak /11 kV RMS

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The STATCOM effectively regulated the bus voltage when required by switching between the capacitive and inductive modes depending on the state of PCC and the control instructions fed into the model predictive controller. The STATCOM initially operates in capacitive mode since reactive power was injected into the grid to restore the bus voltage to its nominal value. At the 0.6 s mark, there was a sudden increase in the bus voltage, requiring the STATCOM to be operated in the inductive mode since reactive power was absorbed to restore the bus voltage to its nominal value.

In another simulation, in order to establish the effective performance of the FCS-MPC controlled STATCOM, without the injection of the FCS-MPC controlled STATCOM, the grid was subjected to a voltage swell from 0.98 s to 1.0 s. At 1.0 s, it was subjected to a voltage sag. The result obtained at the PCC is presented in Figure 16. With the insertion of the FCS-MPC-controlled STATCOM, the grid was subjected to the same disturbances. The waveform of the current injected by the FCS-MPC-based STATCOM and the waveform of the voltage obtained at the PCC of the network are presented in Figures 17 and 18, respectively. Figure 19 presents the harmonic analysis of the regulated bus voltage, which reveals significant mitigation of harmonics in the bus voltage.
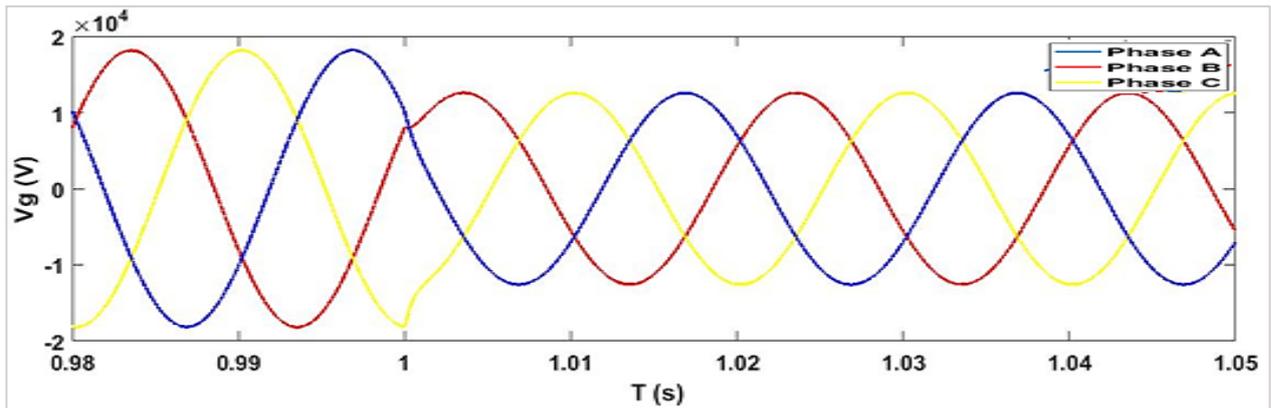

Figure 16: Uncompensated grid experiencing a voltage swell and subsequent sustained under voltage at the PCC
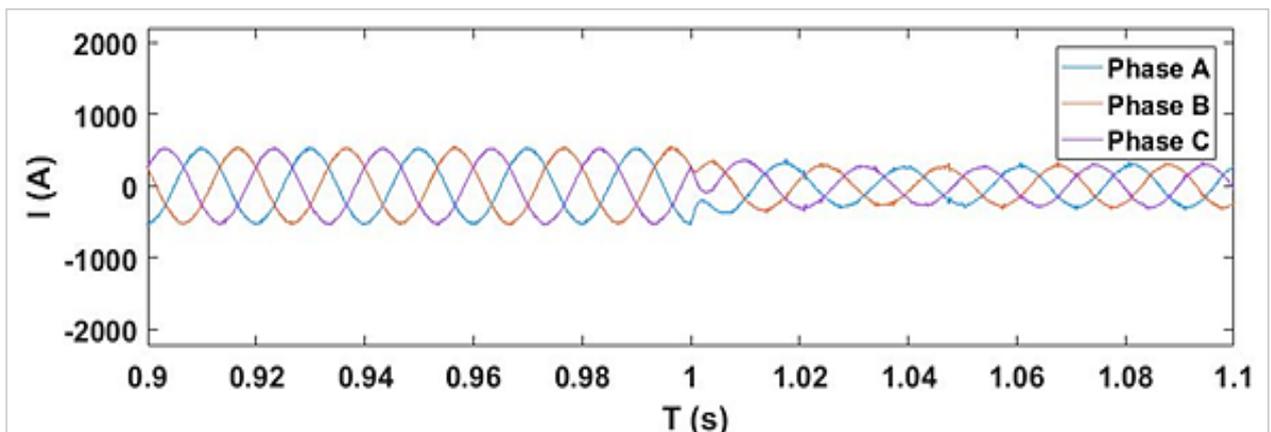

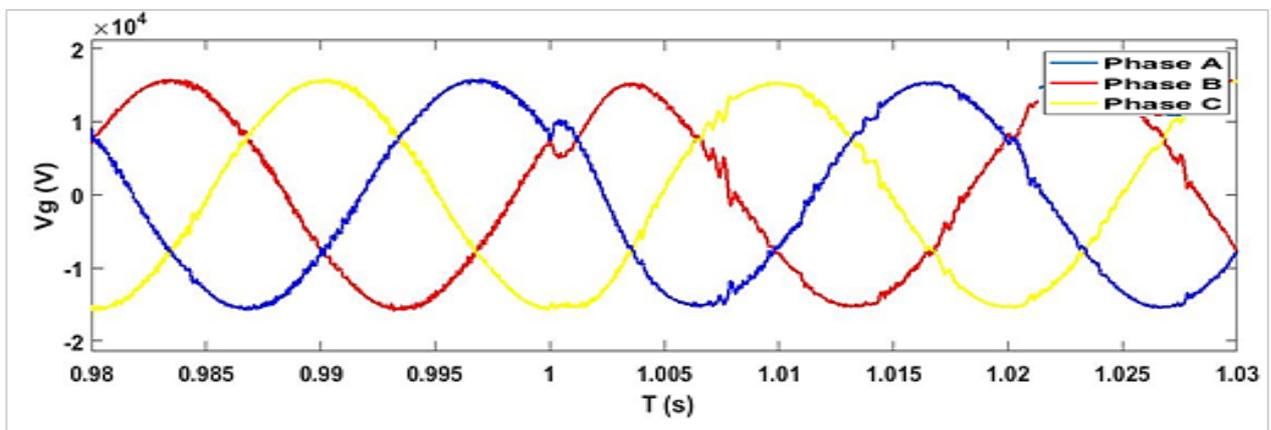**Figure 17:** Injected Current by the STATCOM in Capacitive/Inductive Mode

Figure 18: Compensated grid acted on by the STATCOM to restore the bus voltage to 15.6 kV Peak /11 kV RMS
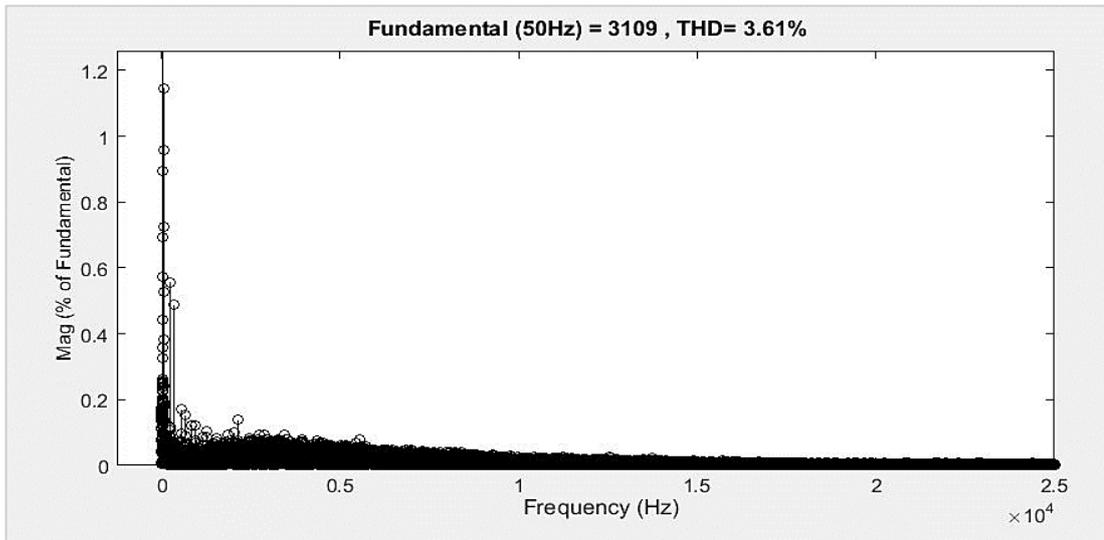
Figure 19: Harmonic analysis of the regulated bus voltage

It should be stated here that the bus voltage regulation was made possible by FCS–MPC, which promptly mitigated imposed disturbances on the test grid based on the established control laws while retaining its stability. The DC link was controlled, as shown in Figure 20. In response to voltage sags and swells, it reacted either by dropping or increasing its voltage; however, the DC link controller ensured that it was restored to its nominal value of 6000 V in 0.3 seconds. The current components, Id and Iq are shown in Figures 21 and 22, respectively. Therefore, it can be stated that the FCS-MPC tracked its references acquired from the two PI controllers controlling the DC link and AC voltage.
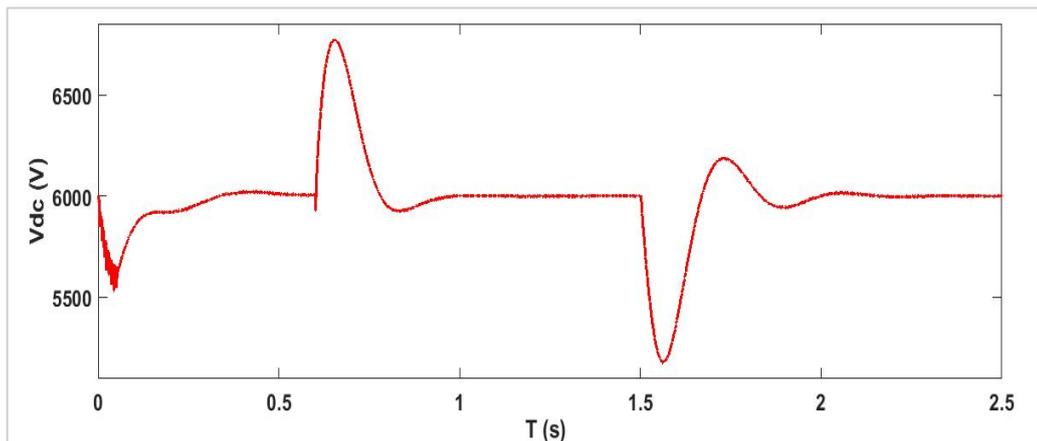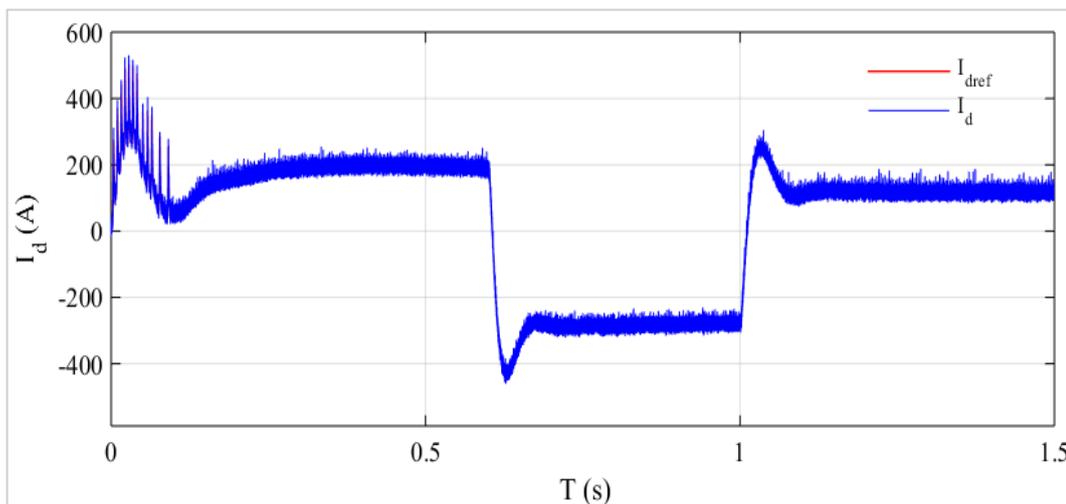

Figure 20: Controlled DC Link at 6000 V

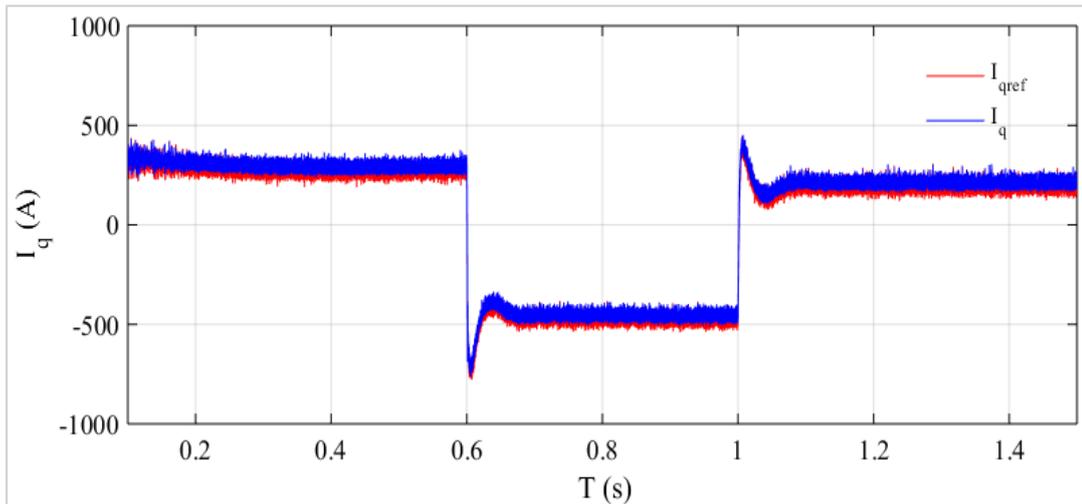**Figure 21:** I_d Component of the FCS-MPC Current Controller

Figure 22: I_q Component of the FCS-MPC Current Controller

9. Conclusion

A model predictive controlled STATCOM connected to the grid through an LC filter has been designed for bus voltage regulation. The gains of the PI controllers for regulating the DC input voltage to the STATCOM and the magnitude of the grid's voltage, which generates the q and d reference currents in the cost function of the MPC, were uniquely selected to compensate for the delays that may destabilize the system. Consequently, the STATCOM effectively regulated the bus voltage when required by switching between the capacitive and inductive modes, as shown in the results. In response to the imposed grid disturbances, the STATCOM mitigated the voltage swell and sag conditions while keeping the THD of the grid voltage within permissible limits. The results obtained from the simulation have shown that the system retains its stability while mitigating against voltage sags and swells at its point of common coupling.

Furthermore, the point of common coupling of the STATCOM to the grid was considered weak, which required a robust PLL that could ride through the grid's inadequacies when the grid's frequency and other parameters were being read. Consequently, the AHPF-DSOGI was developed with correctors for phase and magnitude offsets and introduced to enhance the phase detector of the basic SRF-PLL for grid synchronization. Results obtained indicated significant improvement in the general performance of the AHPF-DSOGI-based PLL over the basic SRF-PLL and improvement in damping overshoot over the improved discrete 3-phase PLL block in SIMULINK.

Nomenclature

v_{iabc}	– STATCOM's inverter output voltage in compact'abc' natural reference frame
i_{abc}	– Filter inductor current in compact'abc' natural reference frame
v_{gabc}	– Primary side voltage of shunt injection transformer at PCC in compact'abc' natural reference frame
i_{gabc}	– Primary side injected current of shunt transformer at PCC in compact'abc' natural reference frame
v_{fabc}	– Shunt filter capacitor's voltage in compact'abc' natural reference frame
i_q, i_d, i_{qd}	– q, d, and complex qd filter inductor currents
i_{qg}, i_{dg}, i_{qdg}	– q, d, and complex qd primary side injected currents at grid
v_q, v_d, v_{qd}	– q, d, and complex qd STATCOM's output voltages
v_q, v_d, v_{qd}	– q, d, and complex qd STATCOM's output voltages
$\boldsymbol{\delta}_{vdc}$	– output of PI controller for DC voltage control
$\boldsymbol{\delta}_g$	– output of PI controller for grid's voltage magnitude
$\omega, \omega e$	– Angular velocity in arbitrary and synchronous frames
r_f	– Output series filter resistance
L_f	– output series filter inductance
C_f	– output shunt filter capacitance
MPC	– Model predictive control
PI	– Proportional plus integral
AHPF	– all high pass filter
DSOGI	– dual second-order generalized integrator
PLL	– phase-locked loop

Author contributions

Conceptualization, A. Balogun.; data curation, A. Balogun and E. Esenwa.; formal analysis, A. Balogun, S. Adetona, A. Olajube.; investigation, E. Esenwa.; methodology, A. Balogun, E. Esenwa, S. Adetona, and A. Awelewa.; project administration, F. Okafor, resources, A. Balogun, S. Adetona and F. Okafor.; software, A. Balogun, S. Adetona, and A. Awelewa.; supervision, A. Balogun, S. Adetona, and F. Okafor.; validation, A. Balogun, S. Adetona and F. Okafor.; visualization, E. Esenwa, A. Olajube and A. Awelewa.; writing—original draft preparation, E. Esenwa and A. Olajube.; writing—review and editing, A. Balogun, S. Adetona, and F. Okafor. All authors have read and agreed to the published version of the manuscript.

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Data availability statement

The data that support the findings of this study are available on request from the corresponding author.

Conflicts of interest

The authors declare that there is no conflict of interest.

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